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Design and modelling of a multi-carrier PWM-based cascaded H-bridge 5-level inverter for a grid connection system

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Abstract
Multilevel inverters typically have lower harmonic content in their output voltage are utilised for high power and high voltage applications. Total harmonic distortion is greatly reduced by multilevel inverters with more levels. Using multicarrier PWM approaches, the output voltage's harmonic content is decreased. MATLAB/SIMULINK is used to create five level cascaded multilevel inverter with multi-carrier PWM approach. The output voltage's total harmonic distortion is verified. Additionally, after adding grid integration requirements, the power flow from inverter to grid is certified and examined using LCL-Filter. Setting the reactive power to zero in MATLAB/SIMULINK, Cascaded Multi-level inverter coupled to a single-phase grid is created to feed the grid.

Key words- Cascaded H-Bridge, Fast Fourier Transform, Total Harmonic Distortion,Pulse Width Modulation, , PQ Control,Modulation Index

1. Introduction

Industry has recently started to require more powerful machinery, which can now produce megawatts of power. A single power semiconductor switch cannot currently be connected to medium voltage grids directly. These factors have led to the development of new family of multilayer inverters as a method of operating at greater voltage levels. The output voltages have more steps when the inverter's level count is increased, creating a staircase waveform with less harmonic distortion. The main PWM method used to drive multilevel inverters is sinusoidal, and a variety of multicarrier PWM methods can be used to reduce harmonic contents[1][4][8]. The basic output voltage is improved and total harmonic distortion is decreased using the multicarrier pulse width modulation cascaded multilevel inverter strategy[2][9].

Additionally, filters must be created in order to lower the system's undesired harmonics[3]. With improved functionality, multilevel inverters are highly helpful in both grid-connected and stand-alone applications[5]. Multilevel inverters have becoming increasingly prevalent in standalone applications, particularly in PV generation schemes. One of the most common inverter topologies used in standalone PV systems is the cascading H-bridge multilevel inverter[6]. Multilevel technology is appealing for PV applications due to the requirement of many sources on the dc side of converter. Because the battery bank is integrated into the topology of the energy storage system, it can operate in either the inversion mode or the battery charging mode. For better use of renewable sources, power generated by wind and solar energy is now connected to the grid. The grid or loads cannot directly use the electricity

generated by renewable energy sources. An interface is employed between them using power electrical devices like DC-AC inverters and DC-DC converters and particularly MLIs. Pure sinusoidal waves or voltage/current with fewer harmonics can both be used to power the grid. The MLI design with LCL filter is used to achieve sinusoidal voltage and current with less harmonics, and the harmonic profile can also be enhanced[7]. Renewable energy sources, such as photovoltaic arrays with DC to DC converters, can provide the MLIs' DC input voltage sources[12].

2.Modelling of Inverters

2.1. Modelling Of Multilevel Inverter Using Pulse Generator

The power industry has shown a great deal of interest in multilayer inverters. In their new collection of features, which are ideal for use in reactive power compensation, they provide a novel approach. A more modern and sophisticated sort of power electronic converter called a multilevel inverter creates a specified output voltage from a number of levels of dc voltages as input. Multilevel inverters come in three different varieties. The first is the diode clamped multilevel inverter. 2. A multilevel inverter with flying capacitors. 3. Multilevel inverter with cascading. Cascaded multilevel inverters are utilised in this project because they require fewer components for each level and ((m-1)/2) H-bridges to build the model.

A single phase full-bridge inverter is connected to SDCS of identical magnitude. Different level inverters' ac terminal voltages are linked together in series. Each inverter level will produce one of three different voltage outputs as -.+ or 0 by combining the four switches, S1 through S4. The ac outputs of the various level full-bridge inverters are individually linked in series so that the resulting voltage waveform is the sum of outputs of all the inverters. The formula m = 2s+1, where s is the total number of DC sources, determines the number of phase voltage levels at the output. There will be two SDCSs and two full-bridge cells in a five-level cascaded-inverter. Five level cascaded inverter's switching table is shown below. In this instance, two full bridges are utilised and connected in a cascade. S_1, S_2, S_3, and S_4 are switches from the upper H-Bridge, whereas S_5, S_6, S_7, and S_8 are switches from the lower H-Bridge. We achieve 5 voltage levels by using the proper switching pattern: 2Vdc, Vdc, 0, -2Vdc, and - Vdc. Here, Vdc equals 100V per. Interfacing with renewable energy sources is the multilevel inverter's most difficult use.

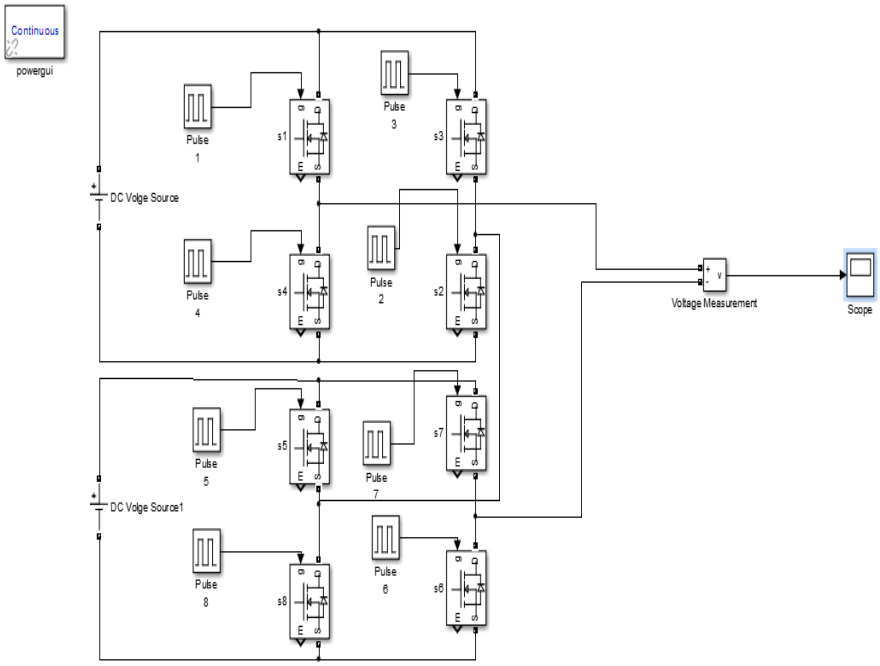

Figure 1. Five-Level Cascaded MLI Using Pulse Generator

Table 1-Five-level cascaded MLI-Switching Table

OUTPUT	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+V_{dc}$	1	1	0	0	1	0	1	0
$-V_{dc}$	0	0	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0
$+2V_{dc}$	1	1	0	0	1	1	0	0
$-2V_{dc}$	0	0	1	1	0	0	1	1

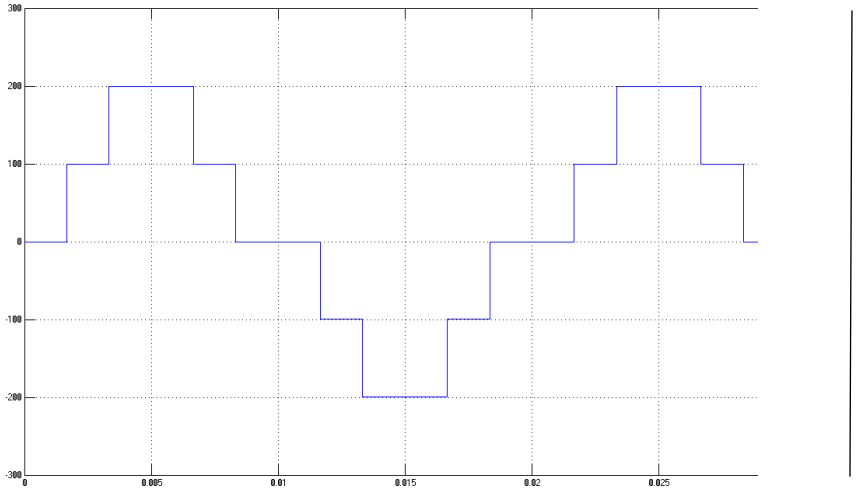

Figure 2. Five-Level Cascaded MLI output Using Pulse Generator

2.2 Modelling of Five Level Cascaded Inverter With Multicarrier Pwm Technique

Pulse-width modulation (PWM) of a signal or power source entails the changing of its duty cycle to either transfer information across a communications channel or regulate the amount of power provided to a load. There are three methods: Phase disposition(PD) the carrier waves collective phase. When compared to reference, all carrier waveforms above it are in phase, and those below it are 180 degrees out of phase (phase opposition disposition, or POD). With respect to its nearby carriers, each carrier waveform is 180 out of phase with them (APOD). This was represented using the PD PWM method.

The DC voltages in the model below are each 100V. The carrier frequency is 5000Hz, while the reference frequency is 50Hz [10,11]. The associated RL type load has values of R=20 and L=47mH, which results in 0.8 PF lagging. By adjusting the amplitude of the reference (modulating wave) signal, the modulation index (MI) in this case can be changed from 0.75 to 1.1.

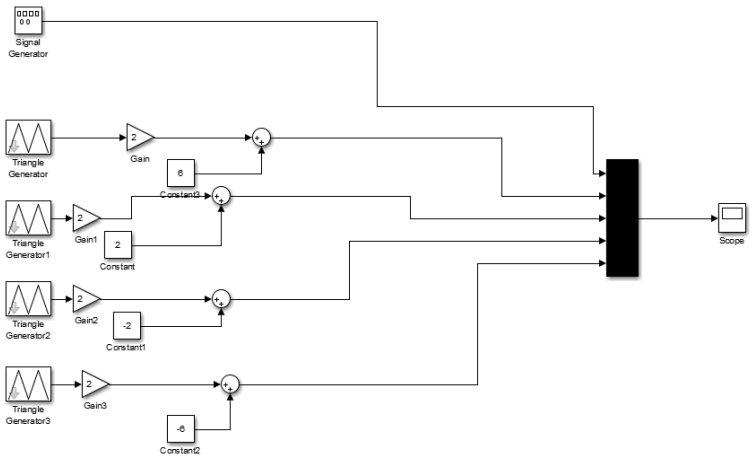

Figure 3. PD multicarrier gate pulse generation

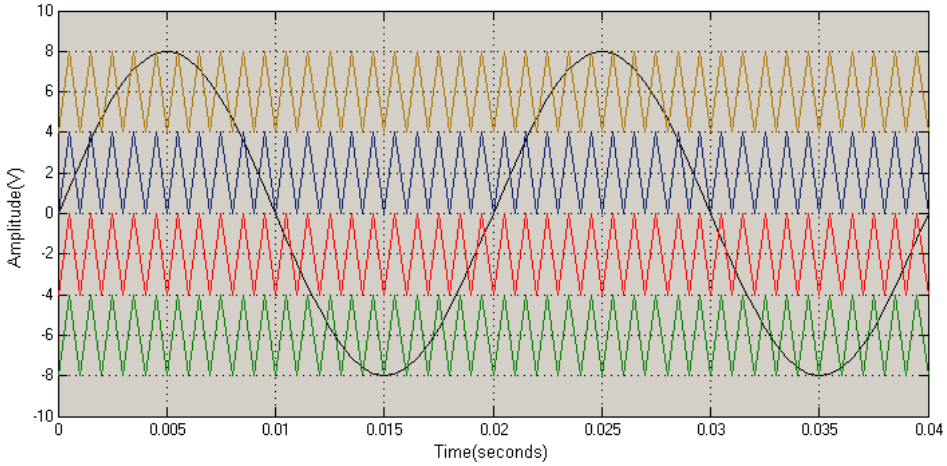

Figure.4. Representation of sine reference and triangular multi-carrier

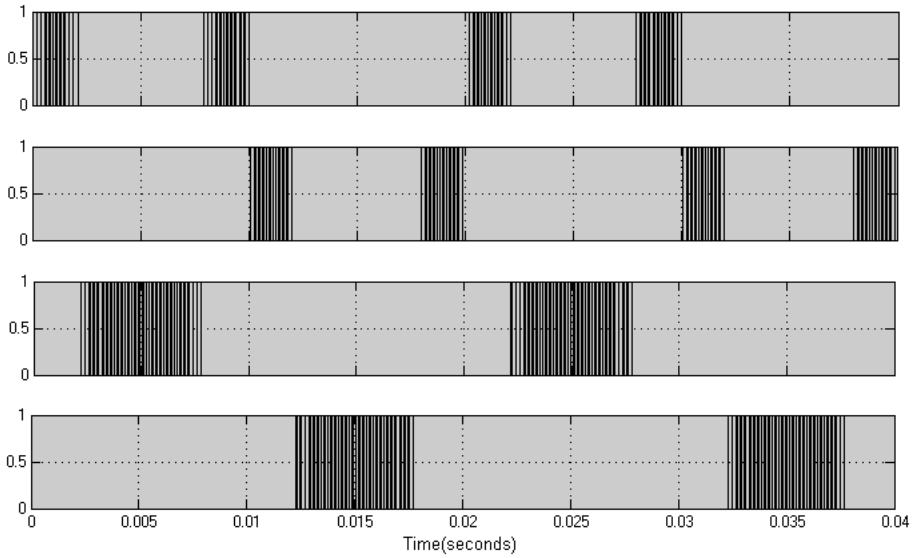

Figure.5. Pulse Generation for 8 switches (with complimentary pairs)

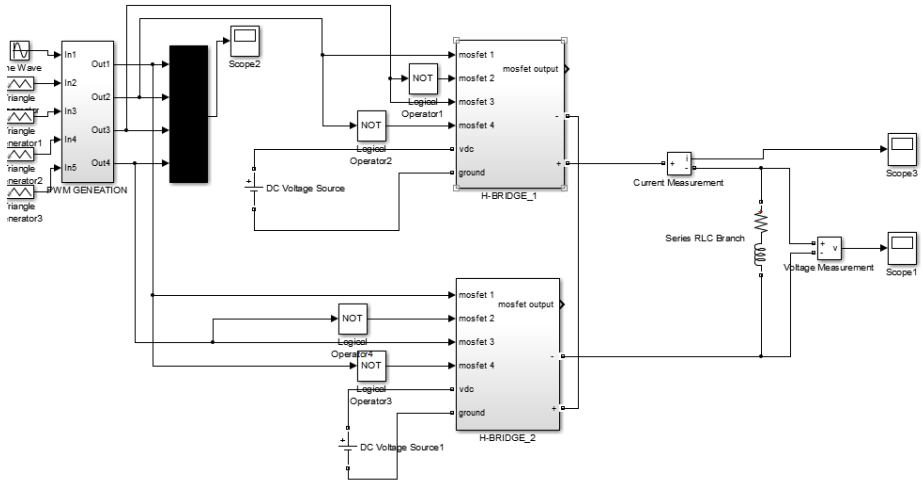

Figure 6. Simulink Model of the Five level cascaded inverter with multicarrier PWM

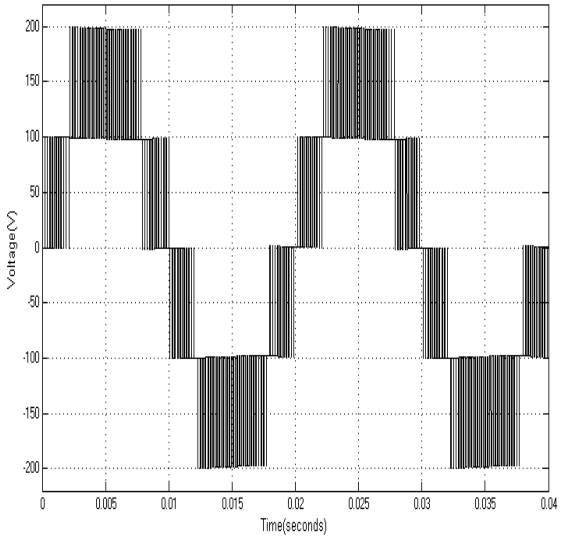

Figure 7. Output Voltage of the Five-level cascaded inverter With MC PWM

3.Discussion

3.1 Exploration of Total Harmonic Distortion Using FFT

Total harmonic distortion (THD) is a performance metric that characterises a waveform's quality. It can be characterised as a measurement of how closely a waveform resembles its essential component. A fundamental wave, which is utilised to perform useful work, and its harmonics, which are variations of the fundamental waveform, produce heat loss in a system [13]. THD is the the mathematical ratio of a waveform's total harmonic content to its fundamental content.

$$\mathbf{THD} = \frac{\sum_{n=2,3..}^{\infty} (V_{on})^{1/2}}{V_{01}}$$

where

V_{on} is the rms voltage of n^{th} order waveform

Where n is 2,3,4……

V_{01} is the rms voltage of fundamental waveform

THD is always 0% for an ideal inverter. Waveform is expressed in fourier series to find the THD,which is as follows:

$$\mathbf{V_{out}=\frac{a_0}{2}+\sum_{n=1,2,3}^{\infty}(a_n \cos n\omega t+\sin n\omega t)} \quad (2)$$

Where,

V_{out-} Fourier series expression of waveform

a_o , a_n, b_n are constants and are defined as,

$$a_0 = \frac{2}{T}\int_0^T V_o(t)dt \quad (3)$$

$$a_n = \frac{2}{T}\int_0^T V_o(t)\cos n\omega t\, dt \quad (4)$$

$$b_n = \frac{2}{T}\int_0^T V_o(t)\sin(n\omega t)\, dt \quad (5)$$

Where,

$V_0(t)$ is the output waveform as a periodic function of time.

T is the Time period of the output waveform.

Reducing the harmonics in the generated current, the output filter lowers the effects of semiconductor switching. Filters come in a variety of forms [14]. Filter inductors attached to the inverter's output are the most basic variation. However, capacitor combinations like LC or LCL can also be employed. LCL high pass filter is utilized in the design, because it attenuates the inverter switching harmonics better than the L and L-C filters. For a 1 KW rated power,LCR filter design values are chosen [15,16].

Table 2 -LCL FILTER DESIGN VALUES

PARAMETERS	**VALUE**
L_i (inverter side)	8.137mH
L_g(grid side)	4.879mH
C_f Filter capacitance	3μF
R_d (damping Resistor)	10.623Ω

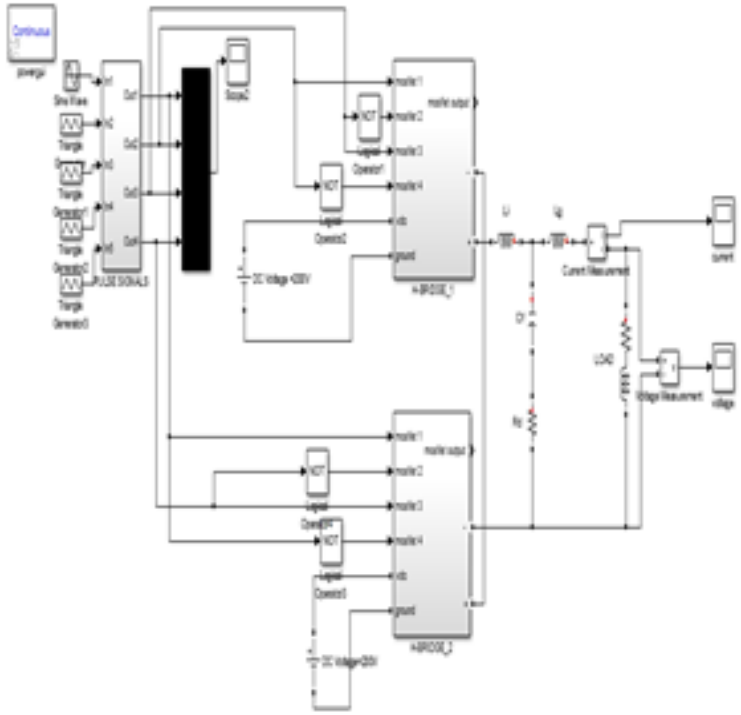

Figure 8. Five-level cascaded inverter with LCL-Filter- Simulink Model

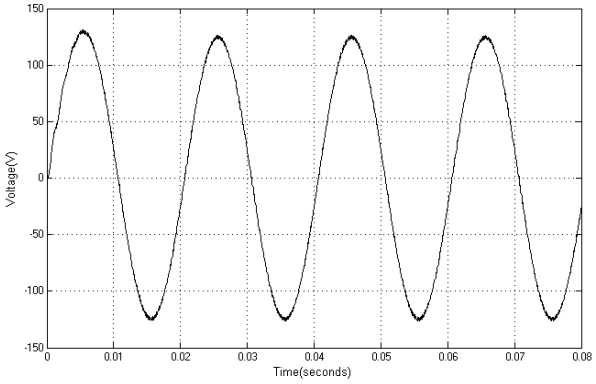

Figure 9. Output Voltage of the Five-level cascaded inverter with LCL-Filter

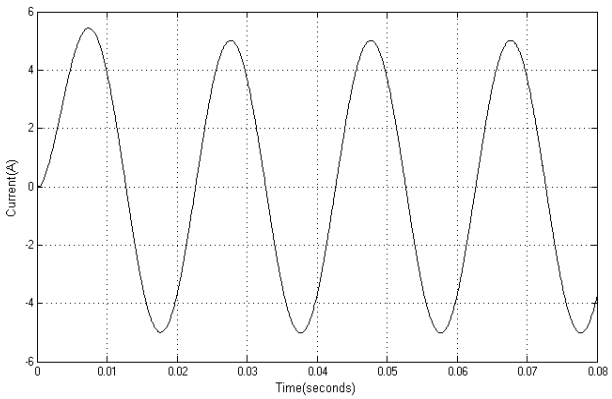

Figure 10. Output Current of the 5-level cascaded inverter With LCL-Filter

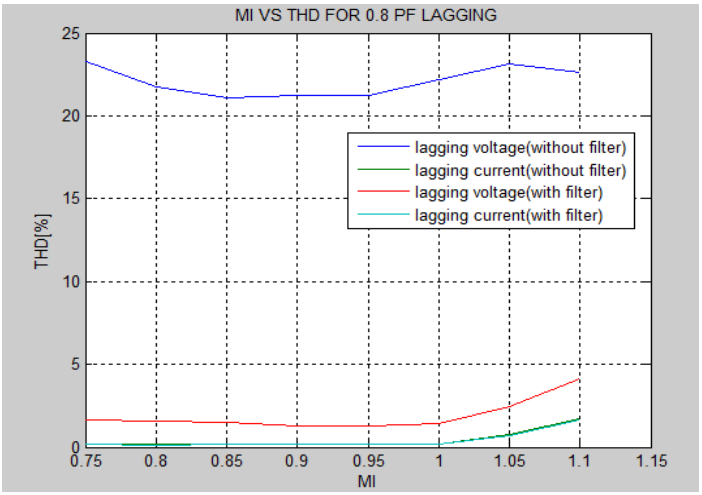

Figure 11. MI VS THD with LCL filter for 0.8 Lagging PF

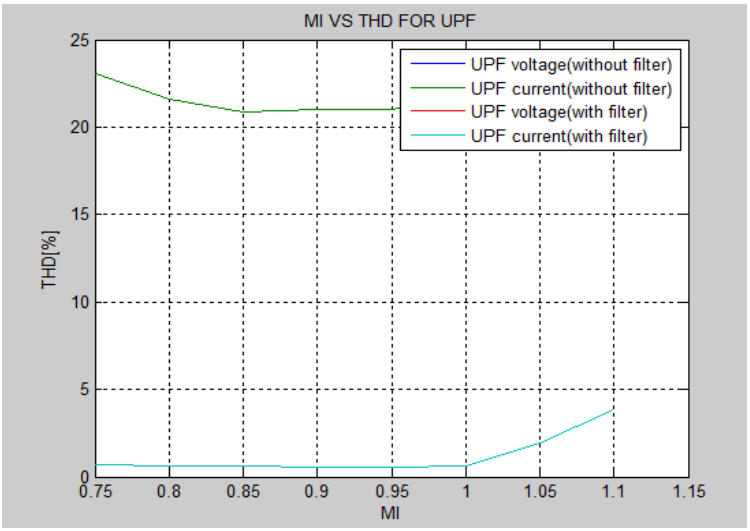

Figure 12.MI VS THD with LCL filter for UPF

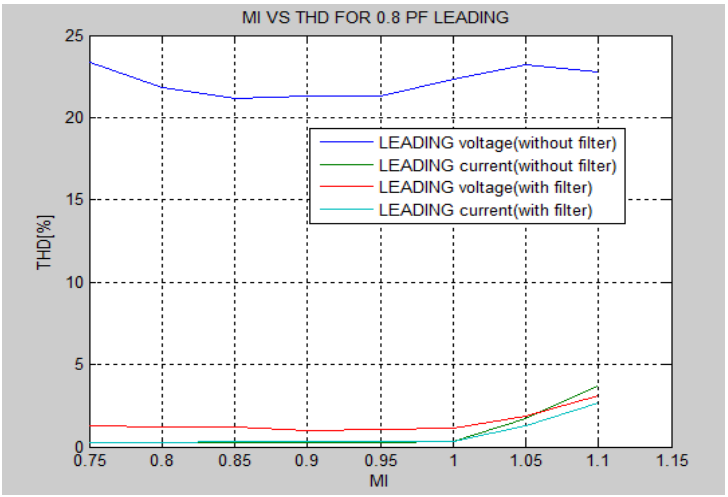

Figure 13. MI VS THD with LCL filter for 0.8 Leading PF

Table 3- THD COMPARISON FOR MI=0.8

LOAD	THD(%) Without filter	THD(%) With filter
R(UPF)	21.60	0.65
RL(LAGGING)	21.78	0.14
RLC(LEADING)	21.85	0.29

4.Results

4.1 Grid Connected Cascaded MLI With LCL-Filter

When integrating the grid, various restrictions are taken into consideration [17]. The L_g inductor in the LCL filter circuit acts as a decoupling inductor, which regulates the power flow from inverter to grid. To allow the grid to receive inverter current, V_{inv} must lead the Vgrid at a specific angle. I_{inv}(Iout) needs to stay in sync with the V_{grid}. This is accomplished by changing the modulating wave's phase angle (reference sine wave). To operate at unity power factor, this is done. (The reactive power is Zero).

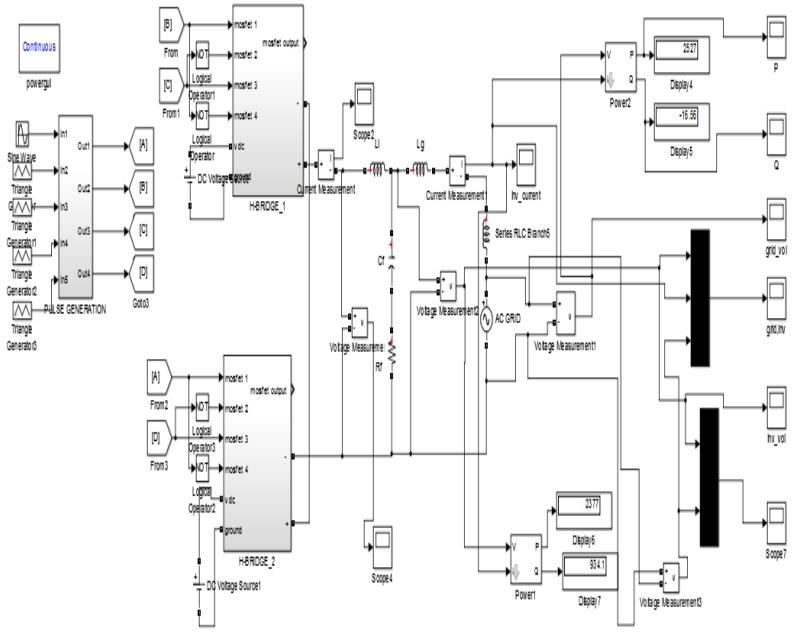

Figure 14. Simulation Model of grid connected cascaded MLI

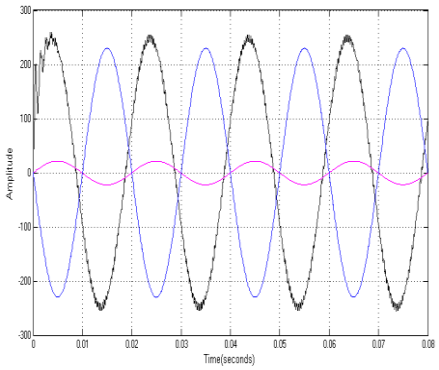

Figure 15. Waveforms of Vinv, Iinv ,Vgrid

From above, it is observed that V_{inv} leads V_{grid} and $V_{grid,}$ I_{inv} are in phase with each other which is the requirement for the power flow.

By using the PI controller tuning [18,19], PQ control is done. The K_p ,K_i values are as follows: 0.001, 0.3 respectively. The real power and reactive power are set to 1000 Watts and 0 Watts respectively.

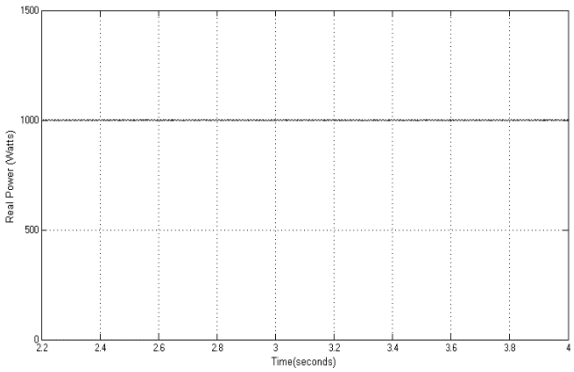

Figure 16. Real power is set to 1000 Watts

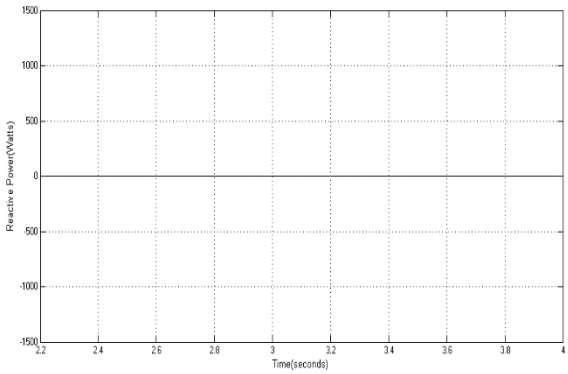

Figure 17. Reactive power is set to 0 Watts

5.Conclusion

The cascaded MLI is modeled with Phase disposition (PD) Multi-carrier pulse width

modulation technique. The harmonic analysis is done and LCL filter is used to reduce the THD. Finally, Grid is connected to the cascaded MLI with suitable constraint enables the inverter output current to flow through the grid. Through phase angle adjustment Unity power factor is achieved in the grid such that reactive power Q=0 is maintained. The PQ control is done using the PI controller tuning in the closed loop domain. The present work can be extended to include PV array as a DC source.

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