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Dynamic Power Reduction Using Switching Activity based Multibit Re-Ordering

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Abstract
In today's application world there is demand of devices which operate on low power, so power is an important sign-off metric. There are many low power techniques like clock-gating, power gating, Dynamic voltage and frequency scaling which are adopted in design flow to help reduce consumption of power by integrated circuits. Multibit banking is a technique where more than one registers having common clock and asynchronous input lines are mapped to one library cell having multiple bits which avoids separate clock and other asynchronous lines. This reduces switching activity and helps reduce dynamic power and area. Use of multibit cells has become part of design flow. This work aims at using multibit in design flow and re-ordering of the bits based on scan switching activity so that bits with low switching activity is used as scan-out of the multibit cell during scan shifting.

Keywords:-multi-bit cell,Power gating, Clock gating, Design-For-Testability, Transition Delay Fault, Memory Built-In Self-Test, Value change dump file (VCD)

I. INTRODUCTION

The growing demand for handheld devices has paved way for packing more gates into integrated circuits and in parallel demanded low power consumption for longer usage of the devices. This is true for every application which process real time data like chips implementing face detection technology where-in the implementing algorithms are more complex. These algorithmsare computationally intensivehaving magnitude of multipliers and adders which undergo lot of switching activity giving rise to power issues. Power issues lead to timing issues and false test failures.

Power consumption mainlydepends on voltage. There are many techniques to reducedynamic power [1] [2][5]. Techniques like clock gating where-in clock lines are made to toggle only when there is change of value on data line reduces dynamic power. There are other techniques like Variable Frequency Islands [3] where not all blocks are clocked simultaneously there by reducing dynamic power. Power gating is also a technique to reduce both static and dynamic power. In a typical application not all design blocks work simultaneously in that case certain blocks which are not functional at a particular time can be switched-off to help reduce power.

It has been proved that there will be huge power consumption during testing [4]. During scan shifting and transition delay

fault testing (TDF), It is observed that all the registers in the design are activated to change the value increasing the power requirements and this test power needs to thoroughly be characterized. Memory testing using Memory Built-In Self-Test(Mem-BIST)involves loadingvariouspatternsatveryhigh-speedincreasingswitching activity within and around the elements requiring higher averageandinstantaneouscurrent. Presence of more memories per controller increases current demand resulting in IR drop causing memory test to fail[6].

High demand of instantaneous current causes wrong value getting captured during manufacturing testing resulting in test-failure and false chip failure which affects the yield.

Multibit cells have more thanonce cell embedded in a single librarycell. Using multibit cells reduces area due to shared transistors and optimized layout. And since clock net length is reduced there will be reduction in dynamic power along with area.

Multibit technology is widely used in today's design flow. Bussed structures in the RTL are mapped to multibit cell during initial mapping and again the registers which are closely placed and share common clock and asynchronous controls like set/reset are remapped to multibit cell reducing area and power. Mapping to multibit cell sometimes comes timing penalty. So intelligent mapping to multibit cells is required to avoid multibit cells on timing critical paths [7].

In design-For-Testability flow, registers will be set to known state using patterns like stuck-at-fault and transition delay fault patterns. This is done using shifting of the data through scan chains. The output of the registers is connected to scan input of next register in the scan chains along with combinational logic and there will be not-needed combinational switching during shifting of scan data. This combinational switching increases dynamic power. There are techniques to reduce the combinational switching such as Q-gatingwhere-in switching of combinational logic is gated using scan control signals during scan shifting [8].

In the flow where multibit banking is employed, regular multibit registers are replaced by scannable multibit registers and in the formation of scan chain, last bit connecting to scan-in of next register could experience more combinational switching resulting in high dynamic power. So, the bits in the multibit can be re-ordered so that bit which experiences less switching activity can be made as last bit of multibit cell feeding the scan-in of next register in a scan chain. Currently the switching activities are computed using statistical methods and there is a need of a methodology which derives more accurate switching activity for the output bits of the multibit cell and re-order the bits accordingly to reduce the dynamic power.

II. DESCRIPTIONOFWORKDONE

The objective of the work is to define a methodology to re-order the bits within multibit cell on scan chain so that bit which experiences lowest switching activity is connected as last bit of multibit cell. A Design size of 500K instances used with 28nm library.

The flow is as below

1. Synthesize the design enabling multibit banking of registers.
2. Perform DFT insertion.
3. Test patterns generation
4. Simulation of the test patterns and switching activity file generation
5. Multibit re-ordering using switching activity information

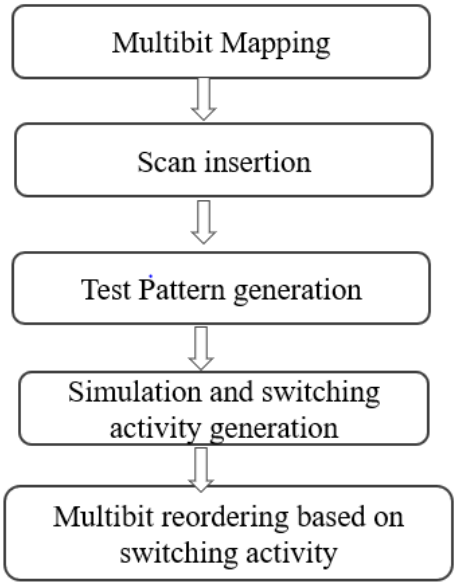

Figure:1 Methodology Flow

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Step1: Multibit mapping: In this step the design is synthesized using industry standard EDA tool using 28nm TSMC library. The input RTL along with basic timing constraints is initially elaborated followed by physical synthesis. Synthesis also involves Design-For-Testability (DFT) logic insertion. Compressor and decompressor logic inserted with compression ratio of 96%. Basic rectangular floorplan is used for physical synthesis. Apart from floorplan, there are some hard macro areas defined for memories. Once synthesis is done and netlist is obtained. Post DFT rule check is performed to verify if the DFT logic inserted is not violating any rules. Timing and power analysis is done at the end of synthesis to analyze the quality of the netlist obtained from physical synthesis.

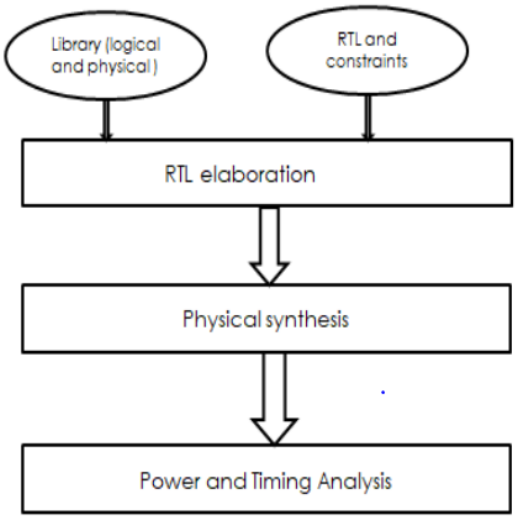

Figure:2Physical synthesis flow

Step2: In this step test patterns are generated for the design synthesized from step1. Industry standard EDA tool is used to generate test patterns. The synthesized design has compressor, decompressor logic. In this work test patterns to target stuck-at-fault (SAF) and transition delay fault (TDF) are generated.

TheTDFpatternistypicallydividedinto3typesofcycles.

1. The shift cycles where input vectors are shifted serially throughflopsviathescanchains.Theshiftingisexpectedto causehighswitchingactivitybutatslowfrequency.
2. One or two dummy cycles before and after shift operationwheretheshiftandfunctionalclocksaredisabled butthescanenablesignaliscontrolledtochangefromtest modetofunctionalmodeandviceversa.
3. Thedummycycleaftertheshiftoperationisfollowed byalaunchcyclefollowedbyacapturecycle.Thesearehigh frequencycycleswheredesignoperatesinafunctionalmode. InTDFtestingonlyoneofthefunctionalclockdomainsis activemostofthetimelimitingswitchingactivityduringthe capturecycle.

Thefollowingillustrationshowshowvariouscyclesare arrangedinaTDFpattern.

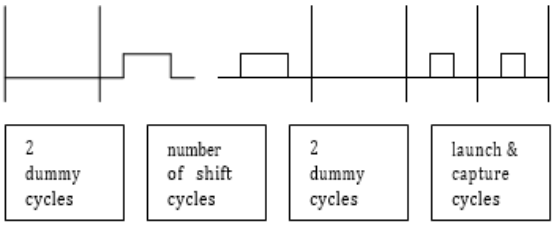

Fig. 3. A typical TDF Pattern

Since multibit mapping is enabled, scan chains will have multibit registers as below

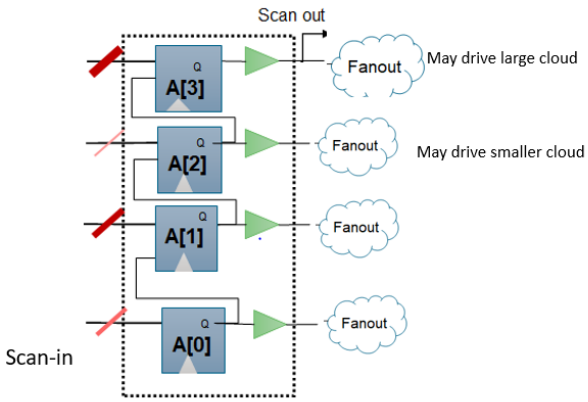

Figure4: Multibit cell on scan chain.

As observed from the figure above bit A[3] is connected to scan-out driving next scan cell and also to combinational cloud and during scan shifting last scan cell A[3] drives both next scan cell and combinational logic. If the combinational logic is large and it may lead to more switching and more dynamic power.And we can see A[2] is driving small combinational cloud which leads to less switching and less dynamic power.

So if we re-order bits so that A[2] drives last scan cell as shown below, we can save dynamic power during scan shifting.

There are existing methods in industry to re-order the bits depending on activity computed based on statistically computation. But in this work, we define a methodology to compute the real switching activity based on simulation

of test patterns.

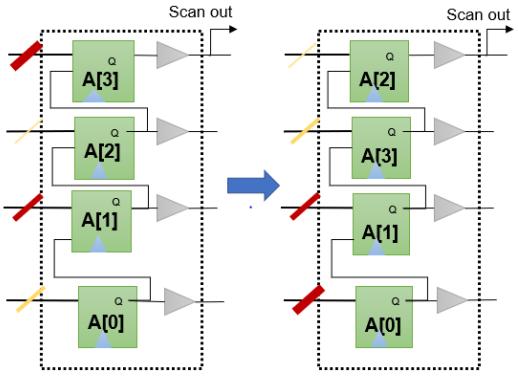

Figure 5: Multibit cell before and after re-ordering

Step 3: In this step Test patterns are simulated using EDA simulation tool. As discussed in step 2, stuck-at-fault (SAF) and Transition-Delay-Fault (TDF) patterns are generated. Here we select 20 top TDF patterns are selected for simulation which result in high activity. The activity on the nets is captured in Value Chane Dump (VCD) file. The VCD file generated is parsed using TCL script to find net activity on the scan-outs of each bits of multibit cells in scan chain. Basically a multibit scan cell is selected and from the VCD file, the activity for each bit is computed and stored.

The bit experiencing lowest switching activity will be connected to scan-out of the multibit cell so that bits are re-ordered to reduce dynamic power.

Input: Design, VCD file
Output: Design with re-ordered Multibit cells

```
foreach o/p bit of multibit cell {
    Find-out net
     Foreach net {
          Calculate switching activity
Store;
   }
     Find the net with low switching
     Connect to scan-out
}
```

Algorithm: re-ordering based on switching activity

Step 4: From previous step, design is multibit re-ordered using the real switching activity.In this step we performed timing and power analysis of the design with and without multibit re-ordering

Metric/Flow	Without Reorder	With Reorder	%Improvement
Dynamic Power	44mW	38mW	13

Area	10203356	10233560	~0
Worst negative slack	-0.007	-0.007	0

III. Conclusion

From the results we could observe when the bits of the multibit cell are re-ordered and compared to run where there is no re-ordering

1. There is reduction in dynamic power
2. No change in area and worst negative slack

In this work only 20 top TDF patterns are chosen to prove the concept of the methodology that real switching activity could be considered to re-order the bits of multibit to reduce dynamic power during scan shifting. A broader EDA solution can be developed based on the work done.

IV REFERENCES

1. Deepak Kumar and Naveen Tiwari,"VLSI designs for low power applications Intl J Engg Sci Adv Research 2015 Mar;1(1):71-75J.
2. Sumita Gupta and Sukanya Padave "Power Optimization For Low VLSI Circuits,Volume 6,Issue 3, march 2016
3. P. Girard, "Survey of Low-Power Testing of LVSI Circuits", in proc. IEEE Design and Test of Computers, May - June 2002
4. Kumar, S. A. S., Naveen, R., Dhabliya, D., Shankar, B. M., & Rajesh, B. N. (2020). Electronic currency note sterilizer machine. Materials Today: Proceedings, 37(Part 2), 1442-1444. doi:10.1016/j.matpr.2020.07.064
5. Mehraj, H., Jayadevappa, D., Haleem, S. L. A., Parveen, R., Madduri, A., Ayyagari, M. R., & Dhabliya, D. (2021). Protection motivation theory using multi-factor authentication for providing security over social networking sites. Pattern Recognition Letters, 152, 218-224. doi:10.1016/j.patrec.2021.10.002
6. Manjunatha V,K Somashekar and N V Babu "Test mode power computation and IR drop analysis of application specific integrated circuits implementing face detection algorithms" 2017, 4th International Conference on Advanced Computing and communication systems
7. Wai Tung Ng, O Trescases "Power management for Modern VLSI loads using dynamic voltage scaling" in proc Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.
8. P. Sreeprakash and M. Hachinger, "A Case Study of IR-Drop in Structured At-Speed Testing", in proc. IEEE Int. Test Conf., 2003, pp. 1098–1104.
9. Manjunatha V, K Somashekar "Power and Performance analysis using multibit technology" in Test Engineering and management Vol 82, Jan/Feb 2020