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Implementation of Low Power High Speed CNTFET Adder Subtractor Circuit

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Abstract
Multi-valued logic design itself is not sufficient to achieve the performance improvement in digital system design in nanotechnology. The need to replace silicon devices with some more efficient new devices are required so as to meet the power improvements in the nanoscale region. Among various devices explored, CNTFET is the most promising alternative to replace conventional MOS transistors. These nano devices have the benefits of low power consumption due to reduced leakage component, ballistic transport operation even at low supply voltages makes them suitable for high frequency and low voltage applications. MVL circuitry has soared in popularity because the threshold voltage of the CNFET device is somewhat adjustable by the diameter of carbon nanotubes. CNFET is used for high performance, high stability and low-power circuit designs as an alternative material to silicon in recent years. Carbon Nanotube Filed-Effect Transistor (CNFET) is one of the promising alternatives to the MOS transistors. The geometry- dependent threshold voltage is one of the CNFET characteristics, which is used in the proposed design. In this paper, we present a novel high speed Adder-subtractor cell using CNFETs based on XOR gates and multiplexer. Proposed design uses fourteen transistors, ten for full adder and four to modify the cell for subtraction. Simulation results show significant improvement in terms of delay and area saving with respectively compared to the latest design. Simulations were carried out using HSPICE based on CNFET model with optimized design parameters. All designs are simulated at 32nm CNFET with HSPICE. The simulation results show that on average, speed enhancement and area saving of 48% and 11% can be achieved with optimized parameters design over default values of these parameters. The cumulative benefits of the novel adder-subtractor design based CNFET result in an PDP reduction by a factor of 41%.

Key Words - Low Power, CNTFET, ADDER, SUBTRACTOR, PDP.

1. Introduction

The Arithmetic operations are widely used in several VLSI applications such as digital signal processing, image, and video processing and micro-controller based systems. Arithmetic operations mainly comprise of addition, subtraction and multiplication.The addition operation is the basic module which is repeated several times to make any complex systems. In recent literature, existing ternary adder and multiplier designs, exploits various approaches. In the first approach,

combinational circuits such as ternary to binary decoder, binary to ternary encoder, binary and ternary logic gates are utilized to implement the ternary full adder designs. That is, in the first stage decoder circuit is used to perform the conversion of ternary input signals to binary inputs, then all the computations are done on decoded binary values and finally binary to ternary conversion is performed using encoder circuit. A CNT structure is made by rolling one or more graphite sheet layers along a wrapping vector. This wrapping vector is decided by the chirality vector(n1,n2) which in turn controls all the electrical characteristics of the CNT device. Ternary logic is a multi-valued in which the third significant value is acquainted with the binary logic. It allows 3 significant voltage levels of 0, 1 and 2 and the corresponding supply voltage values considered are 0,*Vdd*/2 and *Vdd*.The default value of *Vdd* considered here is 0.9 which is the standard value taken for the CNTFET Stanford model. The history of carbon nanotubes is not entirely clear even for those in the science therefore giving proper credit to the person that invented the carbon nanotube has been the subject of several high tech debates among the scientific communities.

The initial history of nanotubes started in the 1970s. A preparation of the planned carbon filaments was completed by Morinobu Endo who was earning his Ph.D. at the University Of Orleans, France. The growth of these carbon filaments were initially thought to be the first carbon nanotubes. However, they failed to meet the measurement requirements for width and thus were deemed, eventually, barrelenes.

This was still a highly important development in the history of carbon nanotubes, but it just wasn't the right time to be considered the first recognized invention.

The first observation of the multiwalled carbon nanotubes was credited to Iijima.

There are some that hold the belief that in the 1950s there was an initial discovery of what could have possibly been seen as the first carbon nanotubes had Roger Bacon had the high powered electron microscope that would have been necessary.

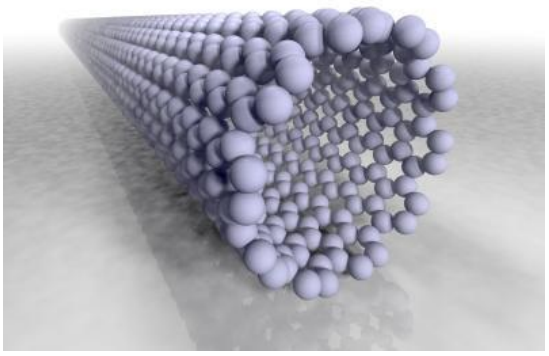

Fig 1: Carbon Nano tube structure

It would be in 1993 that Iijima and Donald Bethune found single walled nanotubes known as buck tubes. This helped the scientific community make more sense out of not only the potential for nanotube research, but the use and existence of fullerenes. With this information, the complete discovery of carbon nanotubes was realized and Iijima and Bethune were ultimately credited with their discovery in their entirety. Russian nanotechnologists were independently discovering the same visual affirmation. They were just a little bit later in their announcement and the potential effect of this discovery. The continuation of research revealed a great deal about nanotubes and

their place in scientific discovery. The research has indicated that there are three basic types of nanotubes (zigzag, armchair, and chiral) as well as single walled and multiwalled nanotubes. There are Bucky tubes, which are completely hollow molecules that are crafted from pure carbon and are bonded together in a pattern of specific hexagon patterns. The multiwalled nanotubes are likely to suffer from defects. These defects happen in more than half of all multiwalled nanotubes. The multiwalled nanotubes have already made appearances in practical applications like creating tennis rackets that are stronger than steel but are ultra-light in weight. These nanotubes are also responsible for creating sunscreen and other skin care products that are clear or able to be blended into the skin without leaving behind residue as well as the creation of UV protective clothing. As nanotechnologists continue to research nanotubes, there is still a race to discover something new within the science. Scientists are researching the potential for life saving techniques as well as the potential to create nanotubes that can be tailored toward specific designated jobs. With the creation of specified nanotubes, the potential for their use will become unlimited and there will be a nanotechnology world hard at work crafting all kinds of products from the convenient to the lifesaving. While might not have been completely aware of the impact his discovery had on the scientific world, he is technically the first scientist to discover these hollow tubes of carbon that are changing lives on a daily basis. Since the initial rediscovery of the nanotubes in 1991, who discovered carbon nanotubes is no longer as important as who can come up with the most practical applications. The nanotube is a molecular structure that can be manufactured, or discovered. In reality, the nanotube is invariable and cannot be anything other than a hollow tube of carbon that remains within the specified single molecule width requirement. With its invariability comes the potential for scientists to create a wide variety of practical applications by testing their potential for directivity and versatility.

STRUCTURE OF SINGLE WALLED TUBES

The structure of an ideal (infinitely long) single-walled carbon nanotube is that of a regular hexagonal lattice drawn on an infinite cylindrical surface, whose vertices are the positions of the carbon atoms.[2] Since the length of the carbon-carbon bonds is fairly fixed, there are constraints on the diameter of the cylinder and the arrangement of the atoms on it.

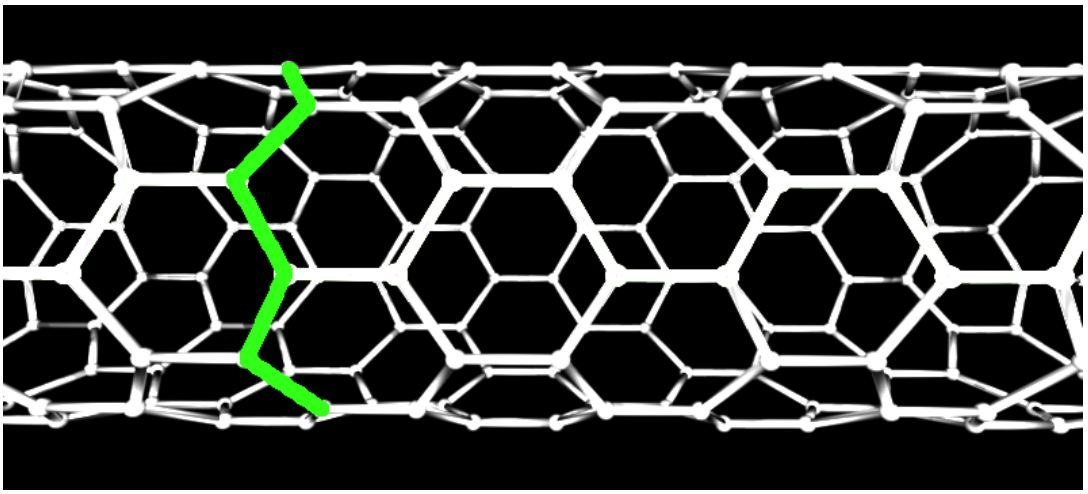

Fig 2: Structure of zigzag nanotube.

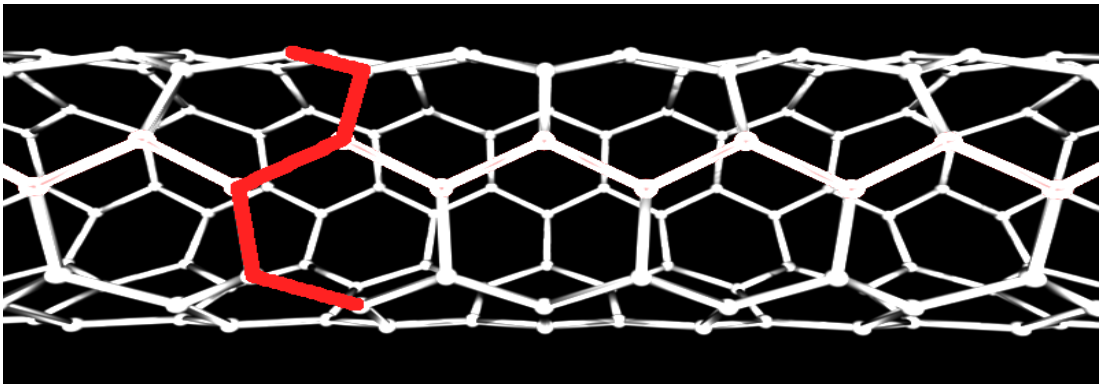

Fig 3: Structure of arm chair nanotube.

An infinite nanotube that is of the zigzag and armchair type consists entirely of closed zigzag paths, connected to each other.

THE (*N*,*M*) NOTATION

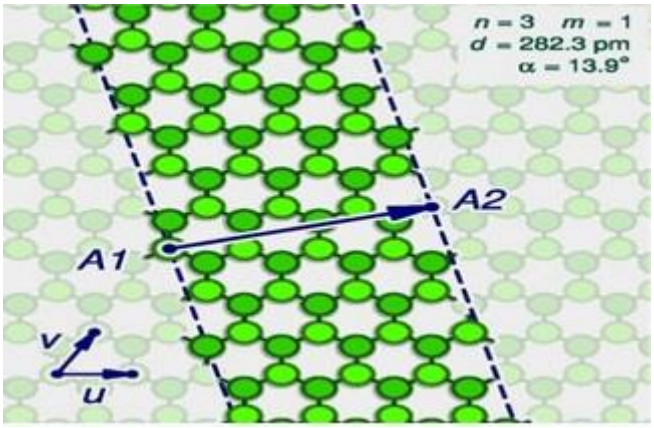

Fig 4: Sliced Representation of Carbon Nanotube

A "sliced and unrolled" representation of a carbon nanotube as a strip of a graphene molecule, overlaid on diagram of the full molecule (faint background). The arrow shows the gap *A2* where the atom *A1* on one edge of the strip would fit in the opposite edge, as the strip is rolled up. The zigzag and armchair configurations are not the only structures that a single-walled nanotube can have. To describe the structure of a general infinitely long tube, one should imagine it being sliced open by a cut parallel to its axis, that goes through some atom *A*, and then unrolled flat on the plane, so that its atoms and bonds coincide with those of an imaginary graphene sheet—more precisely, with an infinitely long strip of that sheet. The two halves of the atom *A* will end up on opposite edges of the strip, over two atoms *A1* and *A2* of the graphene. The line from *A1* to *A2* will correspond to the circumference of the cylinder that went through the atom *A*, and will be perpendicular to the edges of the strip. In the graphene lattice, the atoms can be split into two classes, depending on the directions of their three bonds. Half the atoms have their three bonds directed the same way, and half have their three bonds rotated 180 degrees relative to the first half. The atoms *A1* and *A2*, which correspond to the same atom *A* on the cylinder, must be in the same class. It follows that the circumference of the tube and the angle of the strip are not arbitrary, because they are constrained to the lengths and directions of the lines that connect pairs of graphene

atoms in the same class.

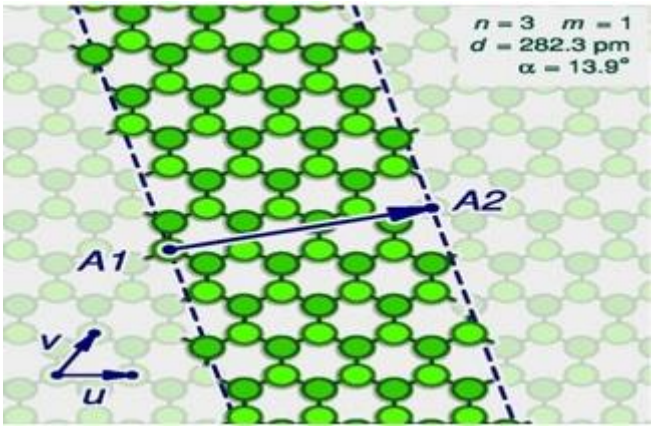

Fig 5: U-V characteristics

The basis vectors ***u*** and ***v*** of the relevant sub-lattice, the (n, m) pairs that define non-isomorphic carbon nanotube structures (red dots), and the pairs that define the enantiomers of the chiral ones (blue dots). Let *u* and *v* be two linearly independent vectors that connect the graphene atom *A1* to two of its nearest atoms with the same bond directions. That is, if one numbers consecutive carbons around a graphene cell with C1 to C6, then *u* can be the vector from C1 to C3, and *v* be the vector from C1 to C5. Then, for any other atom *A2* with same class as *A1*, the vector from *A1* to *A2* can be written as a linear combination$nu + mv$, where *n* and *m* are integers. And, conversely, each pair of integers (*n*, *m*) defines a possible position for *A2*. Given *n* and *m*, one can reverse this theoretical operation by drawing the vector w on the graphene lattice, cutting a strip of the latter along lines perpendicular to *w* through its endpoints *A1* and *A2*, and rolling the strip into a cylinder so as to bring those two points together. If his construction is applied to a pair (*k*, 0), the result is a zigzag nanotube, with closed zigzag paths of 2*k* atoms. If it is applied to a pair (*k*, *k*), one obtains an armchair tube, with closed armchair paths of 4*k* atoms.

NANOTUBE TYPES

Moreover, the structure of the nanotube is not changed if the strip is rotated by 60 degrees clockwise around *A1* before applying the hypothetical reconstruction above. Such a rotation changes the corresponding pair (*n*, *m*) to the pair (−2*m*, *n*+*m*). It follows that many possible positions of *A2* relative to *A1* — that is, many pairs (*n*, *m*) — correspond to the same arrangement of atoms on the nanotube. That is the case, for example, of the six pairs (1, 2), (−2, 3), (−3,1),(−1,−2), (2,−3), and (3,−1). In particular, the pairs (*k*, 0) and (0, *k*) describe the same nanotube geometry. These redundancies can be avoided by considering only pairs (*n*, *m*) such that $n > 0$ and $m \geq 0$; that is, where the direction of the vector *w* lies between those of *u* (inclusive) and *v* (exclusive). It can be verified that every nanotube has exactly one pair (*n*, *m*) that satisfies those conditions, which is called the tube's type. Conversely, for every type there is a hypothetical nanotube. In fact, two nanotubes have the same type if and only if one can be conceptually rotated and translated so as to match the other exactly. Instead of the type (*n*,*m*), the structure of a carbon nanotube can be specified by giving the length of the vector *w* (that is, the circumference of the nanotube), and the angle α between the directions of *u* and *w*, which may range from 0 (inclusive) to 60 degrees clockwise (exclusive). If the diagram is drawn with *u* horizontal latter is the tilt of the

strip away from the vertical.

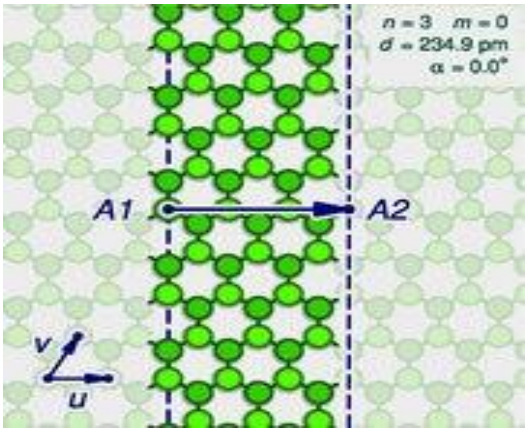

Fig 6: Nano tube of (3,0)

2. Literature Survey

The existing CMOS technology faces numerous critical issues in terms of high power dissipation, short channel effects, and reduced gate control when scaled to nanoscale dimensions. These reliability issues have the tendency to significantly degrade the system performance in the near future. The significant challenge facing the data-processing field is to provide effective technology capable of handling large amounts of data. Currently, semiconductor-based computation is the most used technology for such a task. This computation utilizes binary logic having two values (logic states) for its effective implementation. Several researchers over a period of time have pointed out various limitations of binary logic implementation, with the most significant one being that of the interconnection on chips as well as between the chips. In digital logic circuits, the main source of power dissipation are interconnects, and they occupy about 70% of the active logic elements which are mostly caused by placements of the digital logic components, complex routing, and electrical restrictions which are caused by the increasing number of connections . Full-adder cells are one of the fundamental parts of digital circuits. By putting them together and wiring these cells in the correct way arithmetic circuits like addition, multiplication, division, exponentiation, etc. can be achieved[1, 2]. Various full-adder circuit designs have been proposed by many researchers [3-6]. Implementation of the most full-adder designs has been done by conventional CMOS technology. Nowadays, as the dimensions decreased to nano ranges, designing digital circuits using CMOS technology faced many difficulties such as leakage current in short channel nanometer transistors. It has several types, such as reverse biased diode leakage, sub-threshold leakage, gate oxide tunneling current, hot carrier gate current, gate induced drain leakage and channel punch-through current [7-10].Because of the limitation of CMOS technology, it is achievement of nanotechnology such as carbon nanotube Field Effect transistor (CNTFET). CNFET is one of the several cutting-edge emerging technologies within nanotechnology with high efficiency and a wide range of applications in many different streams of science and technology. Nano-circuits which are based on carbon nanotubes such as CNFETs show big promise of less delay and power consumption than available silicon-based FETs. Many works and circuit designs through CNFET have been proposed by CNFET researchers[11-13].

3. Implementation

ADDER/SUBTRACTORCELL

A binary adder-subtractor is a combinational circuit that performs the arithmetic operation of addition and subtraction with binary numbers. In our proposed design, we developed the full adder cell to operate as an adder or a subtractor. The main idea of our design is implementing multiplexer made of Two pass transistors to choose one among two as shown in Fig. 7. The control line of the multiplexer called the mode M which controls the operation of the adder-subtractor cell. The adder-subtractor cell operates according to the input M. When M=0 the multiplexer select the input B to added with input A so, the circuit performs an addition operation. When M = 1, the circuit add input A and complement of B with one so, it becomes a subtractor. By connecting n-blocks such one-bit Full adders, n-bit ripple adder can be obtained.

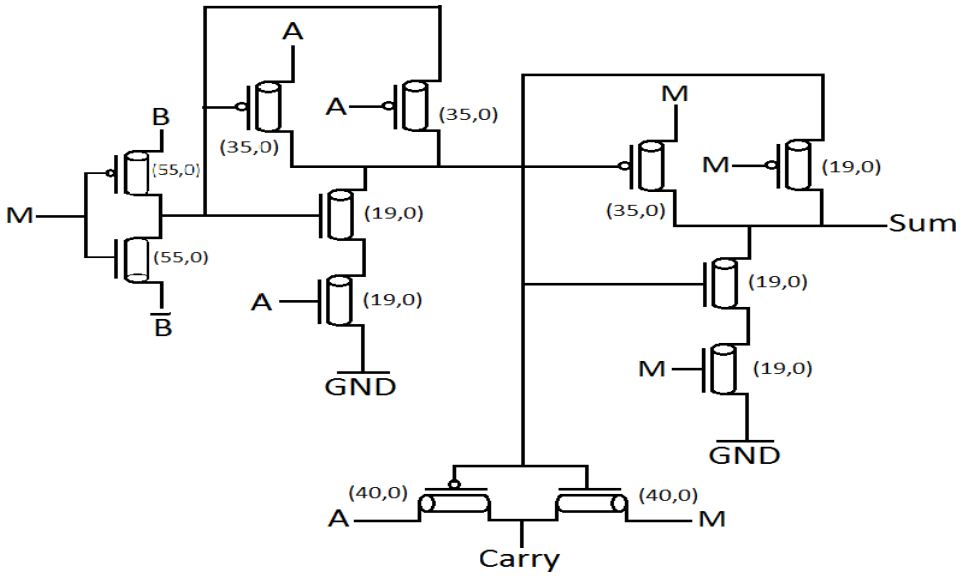

Fig 7: Schematic diagram of proposed adder-subtractor cell based on CNFET

TABLE 1.

	M	A	B	SUM	CARRY
ADDER	0	0	0	0	0
	0	0	1	1	0
	0	1	0	1	0
	0	1	1	0	1
SUBTRACTOR	**M**	**A**	**B**	**DIFF**	**BARROW**
	1	0	0	1	0
	1	0	1	0	0
	1	1	0	0	0
	1	1	1	1	1

TRUTH TABLE FOR ADDER-SUBTRACTOR OF CNTFET

4. RESULTS

In this section, the modified full adder design is compared with the latest full adder design by CNFET. The circuit's are simulated at room temperature and the supply voltage is 0.6V.All designs

are simulated at 32nm CNFET with HSPICE. To verify the output functionality of the novel high speed adder-subtractor circuit, Transient response of the design viewed in Fig. 8. It shows the outputs of bit full adder cell which is completely full swing. 32-nanometre technology node and 0.9 V supply voltage at room temperature is considered, and the analysis is performed using HSPICE simulator.

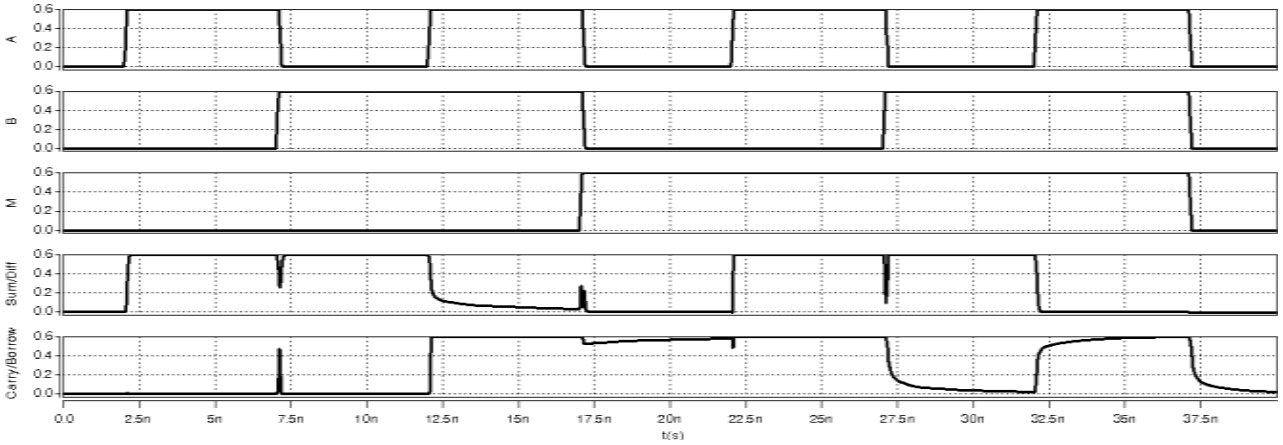

Fig:8 Transient response of proposed adder-subtractor celldesign.

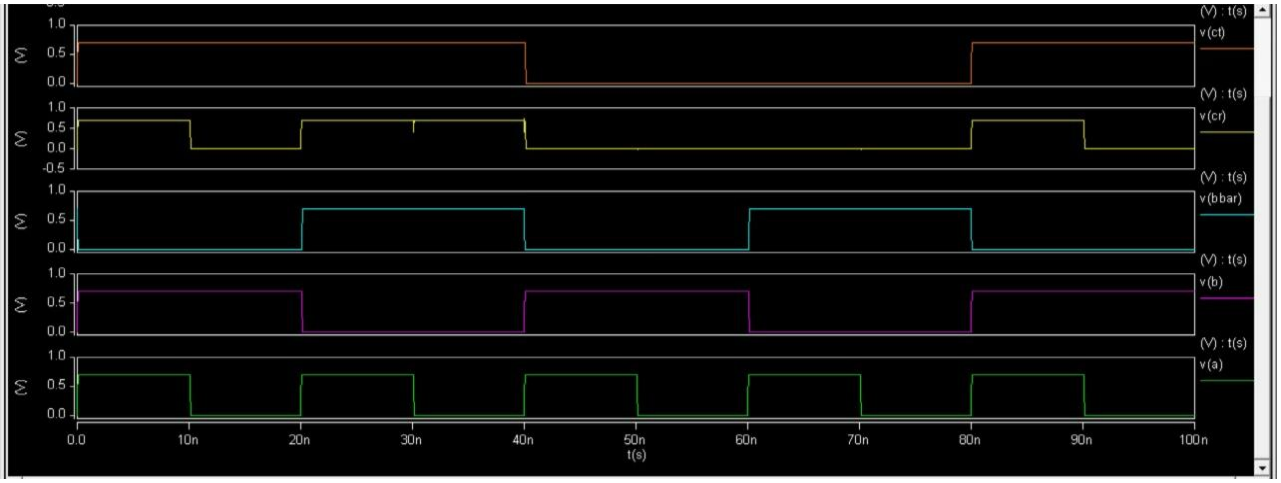

Fig:9 Input Signals of CNTFET

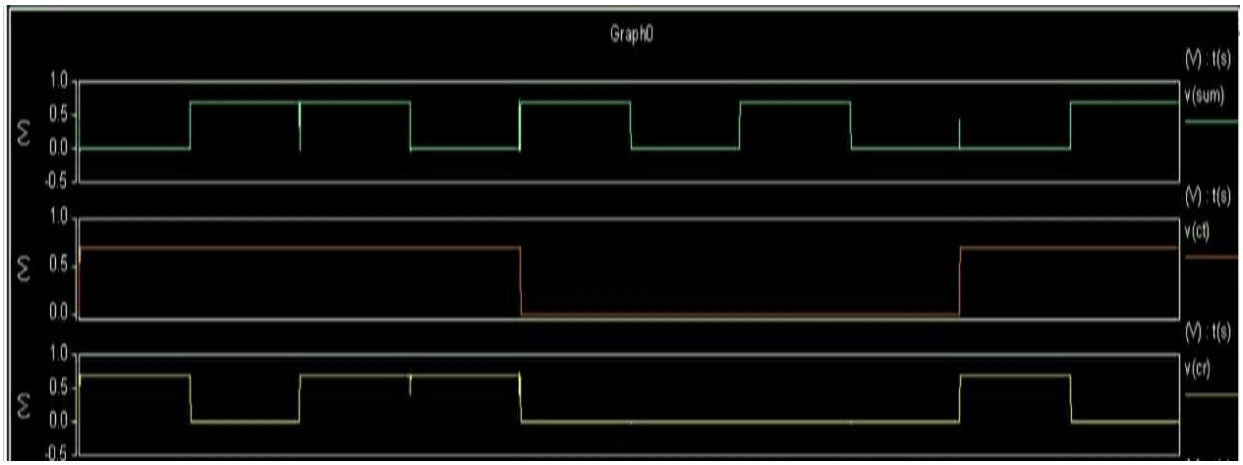

Fig: 10. Output Signals Of Sum and Carry

ADDER-SUBTRACTORCOMPARISON

TABLE-II

Device Used	DELAY sec	AVG.POWER Watts	PEAK POWER Watts
CMOS	3.068e^-11	6.198e^-05	2.477e^-04
CNTFET	1.562 e^-11	4.761e^-08	1.457e^-05

Comparison Table for Adder-Subtractor Of CNTFET

In order to compare more precisely, proposed design is also simulated in different load capacitance as shown in Fig.11 As the load capacitance increases, the delay of the adder-subtractor increases. But the improvement of the speed up for our design is enhanced. Therefore, results show that the proposed adder-subtractor cell has better performance in all situations.

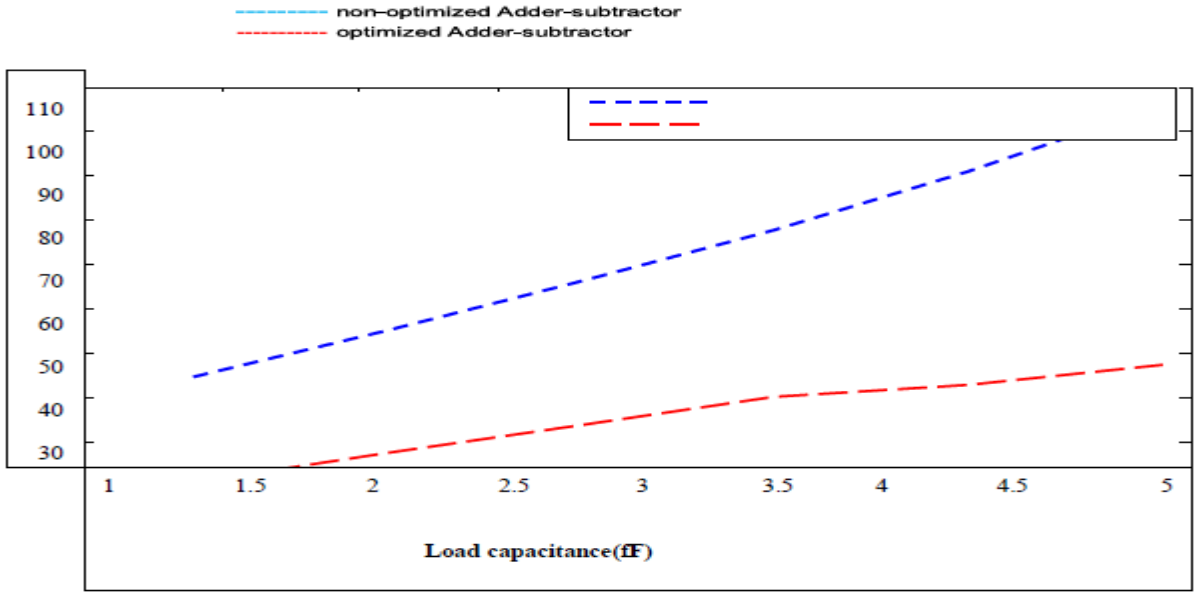

Fig 11 Average delay of Adder-subtractor

5. Conclusion

An improved performance of CNFET Full Adder cell with ten transistors has been presented. The significant improvement is achieved by applying optimized parameters which results in reduction in the delay and area required by CNFET. After that, a novel adder-subtractor design is proposed using CNFET based on XOR gates and multiplexer. Presented design has less number of transistors with high performance for digital circuit design. The simulation results show that on average, speed enhancement and area saving of 48% and 11% can be achieved with optimized parameters design over default values of these parameters. The cumulative benefits of the novel adder-subtractor design based CNFET result in an PDP reduction by a factor of 41%.

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