Increased Clock Gating Efficiency for SRAM and Sequential Circuits

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Abstract
Many different kinds of VLSI architectures find utility in time-critical situations. This study explores several methods for reducing power consumption in VLSI circuits. Combining clock frequency control, switching activity, and scaling factor are just three examples of the many existing methods for conserving power. As glitching and clock triggering difficulties become more common, the suggested study implemented a better clock gating circuit. This work proposes a method for decreasing power consumption through the use of clock gating based on a D-latch model. To reduce clock switching issues like gitching and clocking, a buffer circuit placed between the source and load circuits and integrated clock triggering on the LATCH circuit could be implemented. The SRAM and sequential counter circuits in this implementation are optimized for performance while adhering to the power-decrease method. Many practical uses rely heavily on specialized circuits designed for them, such as FPGAs and DSPs. Power reduction results from SRAM and sequential circuits need to be evaluated through experimental study. As compared to earlier studies, improvements in coverage, power, and latency were achieved. The majority of the design is done in Xilinx 14.2 ISE.

Keywords: Enhanced clock gating; D-Latch gating; SRAM; sequential circuit;Area; Delay;

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Introduction

Reducing power consumption in VLSI circuits is essential for use in real-time applications. Since there are many different ways to perform gate-level switching operations, VLSI circuits consume a lot of energy. Using gate level circuits, one can choose between various logic configurations with respect to power usage. Multiple elements, including as the circuit's power supply, the ambient temperature, and the qualities of the semiconductors, contribute to the overall level of noise in a digital system. An important source of energy loss in a circuit is ground bouncing. It is possible to use channel [1] data transmission limits as an approximation for the minimum allowable power dissipation. In a gate-level circuit, different combinations of lawful gateways can produce the same outputs, but with wildly varying estimates of power consumption [2]. The delay at each bit of data in the gate logic must be ignored if the module's logical utility is to be evaluated. Memory chips can be divided into two categories: static and dynamic [3]. Static RAM relies on flip-flops to store data, while dynamic RAM uses MOSFETs and a capacitor. Preparing sensor node layouts using partitioned SRAM helps meet the low-power criterion as well [4].

The primary objective of this study is to discover new ways of reducing the power dissipation of VLSI circuits, and several reviews have looked into this question. Some methods used to cut down on power waste include increasing voltage, decreasing semiconductor size, and putting semiconductors to sleep. Despite the design's complexity, a 6T SRAM cell was incorporated to provide reliable circuit execution and efficient use of energy. To reduce leakage power with a clock gating technique, [5] DFF with big register circuits on the VLSI module are frequently favored. Clock triggering techniques, switching pulse-based gated clock generation, and a synchronous clock generating circuit [6] have been designed to minimize power consumption. As the power requirements of Static Random Access Memory Field Programmable Gate Arrays (SRAM FPGAs) continue to rise, new CAD tools and lower power FPGA hardware are required. Clock-gating approaches have been implemented in low-force FPGA systems with limited success in lowering total normal force consumption [7]. Clock-gating relies heavily on topological and fractional reconfiguration. The arrangement relies heavily on the successful reconfiguration of design memory to incorporate the clock guiding assets. Using gated, tree-based clock drivers, the D flip-flop lessens the burden on the dynamic clock drivers. Using D flip-flops mitigates clock spikes while also decreasing clock signal power consumption [9]. The DFF is used to control the "CLK" signal's journey from the global clock source to the proximal clock signal in the memory, and the "Lock" signals along this path are dynamic [10]. On the basis of the DFF output and the global clock, an AND-based RTL circuit provides a neighborhood clock signal for memory [11].

Lower power FPGA hardware and new design techniques are required because of the exponential growth in power consumption in SRAM-FPGAs. Implementing clock-gating techniques in low-power FPGAs has been attempted with little success in reducing total power consumption [12]. The clock-gating strategy is predicated on topological shifts and internal reorganization. The problem stems from a missing step in reconfiguring the setup memory diagrams for the clock control resources. The normal power disseminated by the circuits can be determined by observing their motion, which can be used to analyze their performance. Limiting the amount of data that can be exchanged in a VLSI design is one such goal [14]. [15,16]. The DFF's clock gating strategy can be supplemented with logic to infer a gated clock. Delay and power consumption minimization are two primary design objectives [15]. In this case,

retiming could be used to postpone the formation of succeeding circuits. The least spread over a tree for a very large scale integrated circuit can be determined via an RTL computation.

Using the Bellmanford computation, researchers can isolate the synchronous circuitry of the basic way of analysis [16]. Clock gating is generally accepted as the most energy-efficient method due to its ability to cut power usage at the framework, RTL, and gate levels. At the RTL level [17], which is higher than the gate level, tasks are completed in register blocks, much as they would be in a logical gate circuit. Disabling the clock while flip flops are not in use is the fundamental objective of the clock gating technique [18]. The clock gating process can be found in three distinct cell types: those that rely on latches and flip-flops, as well as those that rely on gates. The downside is that the positive edge set off counter has a glitch when the empower signal transitions from 1 to 0 and the clock is on the rising edge [19], [20]. Given that root cause, it stands to reason that the result produced is flawed. When empower is set to 1, the GCLK is put in jeopardy by the instability of this circuit [21]. The increased clock gating technique will be implemented during simulations and synthesis of SRAM and sequential circuits to cut down on leakage power. In a latch-based approach, clock switching activity triggers DFF and logics. Here, the emphasis is on lowering latencies and increasing power efficiency. In this work, static and dynamic power reduction are applied effectively to outperform prior approaches. This section serves as a synopsis of the paper itself. Power efficiency research on very large scale integrated circuits (VLSIs) is the subject of Section II. The proposed logic, along with certain novel and helpful algorithms, are presented in Section III. Section IV presents the results and comments. The rationale and improvements are summed up at the end of section V.

I. LITERATURE SURVEY

Zamin Ali Khan, et al. (2011) has presented the power consumed VLSI design with power optimization approach, which utilized the genetic algorithm. Booth multiplier VLSI design is constructed to test the power by triggering gated switching logic. Here the GA is used to find out the different combination of gates logic onto the power estimation to determine the fitness value; these consequently reduce the power. Benchmark ISCAS-89 circuit is used and performance analysis depends on the gated logics and power consumption on that circuit. Physical design of VLSI circuit utilized the chip analysis and optimization using GA.

Bo-Cheng C Lai, and Jiun-Liang L, (2016) has presented the multiport memory logic on the RAM design with FPGA implementations. The use of Block RAMs (BRAMs) is a basic execution factor for multiported memory plans on FPGAs. Not exclusively does the exorbitant request on BRAMs block the utilization of BRAMs from different parts of a plan, however the complex steering among BRAMs and interconnection likewise restricts the frequency range. This presents a shiny new viewpoint and a more proficient method of utilizing a regular two peruses one compose memory as a 2R1W/4R memory. By abusing the 2R1W/4R as the structure block, this presents a various leveled plan of 4R1W memory that requires 25% less BRAMs than the past methodology of copying the 2R1W module. Recollections with more read/compose ports can be reached out from the proposed 2R1W/4R memory and the various leveled 4R1W memory.

Nandita S, et al. (2015) has presented the clock gating technique on VLSI circuits for power reduction strategy.The framework is a coordination of fundamental structure contains sensor framework, control units into existing power frameworks which could be actualized as Silicon on Chip (SoC) in VLSI circuits. VLSI circuits can be both sequential and combinational. In consecutive circuits, the clock is the significant wellspring of dynamic power utilization. The method of clock gating is utilized to lessen the clock power utilization by removing the inactive clock cycles. VHDL-based strategy, to embed the clock gating circuit and furthermore the unique power because of this is assessed.

C Ashok Kumar, et al. (2020) has presented the loss minimization strategy of VLSI circuits to analyze the power. The solitary chip plannedto reduce low territory frameworks for bringing more proficient gadgets, which are more modest in size. Circuit produced at a very high rate and they devour a space parcel more than they used. The premier worry of VLSI engineers was Area, power performance and Cost. Power has consistently been an optional concern. Latest thing has given more weight to Area, Power and Delay because of versatile specialized gadgets. The high velocity calculation gadgets with complex usefulness are a developing pattern which is request to low power utilization.

Sreenivasulu, et al. (2016) has presented the optimized sequential circuit to reduce the power leakage by multi threshold CMOS circuitry.This method designed to gives lower leakage current and offers upgraded speed. It utilizes low edge voltage gadgets for low leakage and high limit voltage segments as rest semiconductors. These rest semiconductors are sufficient to disconnect the rationale modules from the stock, ground to lessen the spillage current. Furthermore the most un-conceivable time for turn ON state in a circuit is essential worries for power utilization.

Xuan-Thuan N, et al. (2018) has proposed the RAM based content addressable memory architecture on FPGA using hierarchical partitioning approach.In the clock cycle, the update phase of an RAM-based content-addressable-memory consistently endures high idleness. Two essential drivers of such inactivity include: (1) the mandatory eradicating stage alongside the composing stage and (2) the significant distinction in information width between the RAM-based CAM and the advanced frameworks. The design of RAM-based twofold CAM updates the low latency. A few RCAMs, whose information width goes from 8 to 64 bits, were incorporated into a 256-bit framework for the assessment.

Priya Singh and Ravi Goel, (2014) has presented the comprehensive study of power optimization technique in sequential circuit. Here the clock gating is performed to improve the result. Low power VLSI circuit is the most basic issues in the present ASIC plan, as the element size is downsized and there is a pressing requirement for power advancement. Clock gating is perhaps the most rich and exemplary methods for decrease of dynamic influence, significant factor in all out power utilization of any VLSI circuit. Clock gating procedure empowers saving of electrical power utilized by PC processors. It guarantees power saving by turning on a practical logic block clock, yet just when required. The survey of existing clock gating procedures and its focal points furthermore, impediments with a demo of D flip lemon and 4 bit Pseudo Random Binary Sequence Generator.

A Jagadeeswaran, et al. (2012) has presented the optimized power level based sequential pulse triggering approach. Flip-flops are the significant storge components in all SOC's. They oblige the majority of the power that has been applied to the chip. Flip-flop is quite possibly the power utilization parts. It is essential to decrease the leakage power in both clock circulation and flip-flops. The power

delay is principally because of the clock delays. The deferral of the flip-flop ought to be limited for effective usage. This venture moves around in supplanting regular expert slave based on D-FF to a pulse set off flip flop which goes about as a recognition substitute for low power applications. In this, semiconductor sizes and heartbeat age circuit can be further diminish for power saving. Here UMC CMOS 180nm innovation is use in SPICE device to plane for the structure.

II. PROPOSED METHOD

The proposed design of SRAM and sequential counter circuit is used for analyzing the power by using improved clock gating technique. Here the Static Random Access Memory circuit is designed with improved clock gating technique using D-latch based buffer circuitry of gated clock generation to reduce the power dissipation and the counter circuit of sequential logic is designed with improved clock gating technique. The input enabled logic is performed on the register circuits and it is integrated with the improved clock gating technique. In this, the clock and enable signal applied on the gated clock generation module using D-Latch circuit and it is enabled with the AND logic. Based on the triggering state of the clock switching, the gated clock is generated to the SRAM and sequential counter circuits. When the circuit is in idle condition, the clock switching state occurs with triggering problem this causes increased leakage. Therefore, the clock gated switching control based logic is designed to utilize the SRAM and sequential counter logic circuit with improved clock gating technique.The proposed block diagram of power reducing technique of SRAM and sequential circuits are using the improved clock gating technique is given in the figure1.

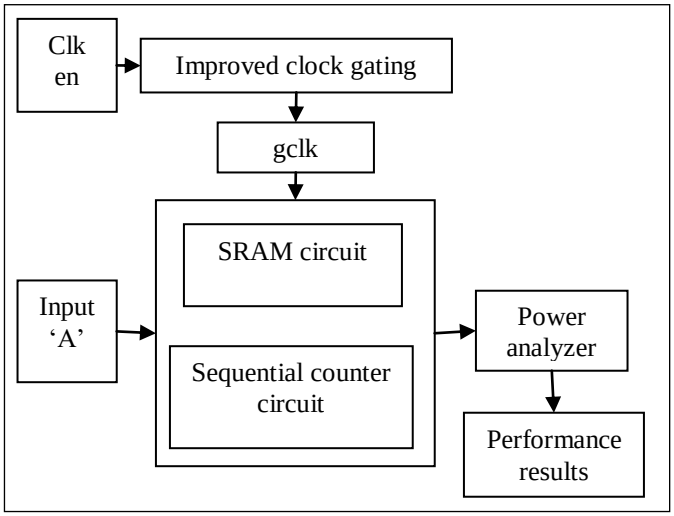

Figure1. Proposed block diagram of power optimized SRAM and sequential circuits

The VLSI circuit optimization involved with various technique for improving the performance. By changing the width and length of the transistor, the minimum impact is possible on the VLSI layout circuit. While connecting source and load impedance, the buffer is used to reducing the number processing stages.

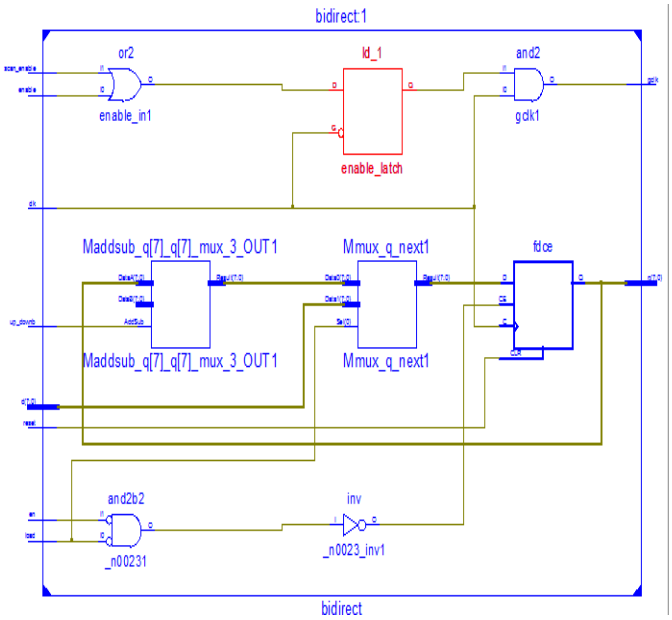

Figure2. RTL view of Bidirectional counter with Improved Clock Gating Technique

The RTL schematic of Bidirectional counter circuit is shown in figure2. The load decoupling is also helpful for reducing the critical path on circuitry. By strengthening the switching activity, the clock signal variation may get better computation. The static power dissipation of CMOS circuit is reduced by capacitance utilization with better transition activity and the pre-charging the higher capacitance to improve the speed.

A. SRAM circuit

Synchronous RAM is designed with the improved logic of gated clock generation circuit to reduce the power leakage. D Latch registry with level delicates the positive lock passes contribution to yield on high stage, hold time on low enable states. Here the positive register tests on rising edge with sample input and the edge triggering is performed with the flip flops. Static power optimization with clock gated signal generation triggers the logic by switching activity and adding of BUFF logic on gclk. Here the Static power of RAM is controlled and optimized the power with effective utilization.

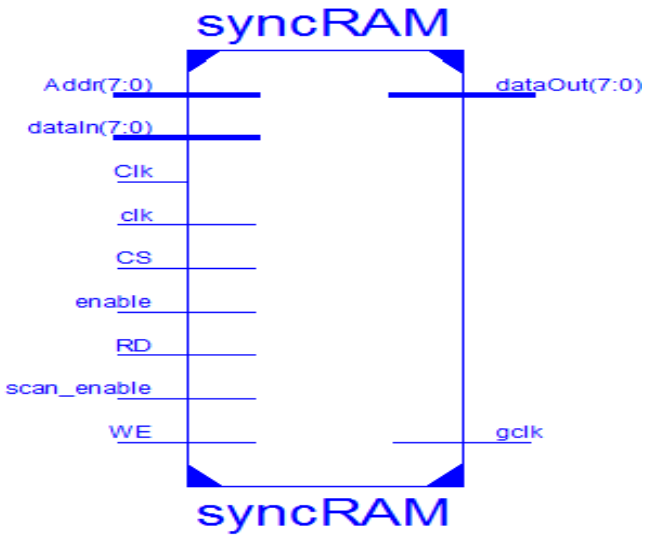

Figure3. SRAM circuit RTL schematic

SRAM logic structure is designed to utilize the clock gating approach with RTL view (see figure3). The clock gating strategy has been created to evade leakage power. When the framework is inactive, the clock switching timing of clock gating is TURN OFF. Explicitly for flip-flops, clock gating implies debilitating the clock signal when the info information doesn't change away the information. It may be applied from the framework level where the whole useful unit can be specifically set into rest mode, or from the sequential circuit level where a few bits of the circuit are in rest mode while the rest of the logic blocks are working. In any case, Clock gating doesn't come free of charge. Additional logics and interconnects are needed to produce the clock empowering signals.

B. Sequential counter Circuit

Sequential counter circuit with bidirectional logic designed with the improved clock gating technique to reduce the power leakage. Here the RTL gate level performance is used for the gated clock circuits to improve the performance. Register with BUFFER utility on D-FF is shown in RTL view (see Figure 4).

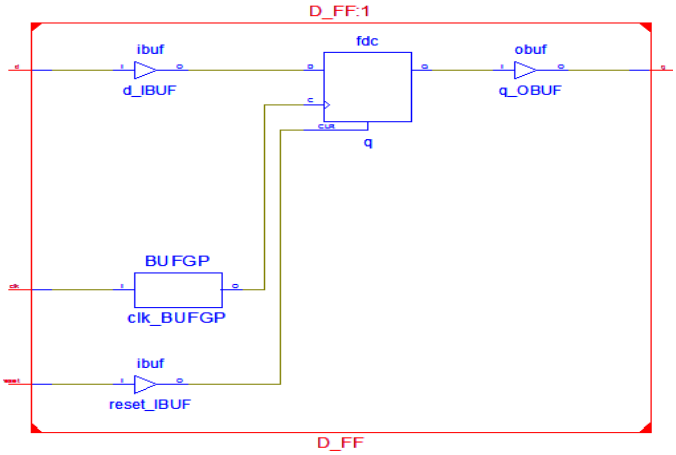

Figure4. RTL view of BUFF added D-FF

Power consumption techniques mainly focus the static and dynamic to improve the performance of VLSI circuits. Aside from this short out and leakage assumes a crucial part in fixing the general energy utilization in a circuit. Static power is because of the quantity of intelligent a part utilized in the module and dynamic happens as aftereffect of number of transient states in the logics. Short circuit flows additionally happen in this situation of when both NMOS and PMOS semiconductors are in ONactive state. Capacitive activity prompts dynamic energy utilization, which is most moving issue to bargain with as exchanging movement is high in consecutive circuits. If the circuit allows for timing logic with switching activity, the clock edges are reducing its existence on precharging state of capacitance.

C. Modified Clock gating technique

At the point when the present and next condition of the D flip failure is noticed, it is seen that when two nonstop information sources are indistinguishable, the D flip failure gives a similar incentive as yield. The clock cycle that is taken care of into the D flip lemon when the yield doesn't shift is named as inactive clock cycles. To eliminate these, at the point when the flip lemon are of various qualities the EXOR entryway passes a yield 1 which is given as a yield to the AND entryway alongside a clock beat gave to the flip lemon for additional exchanging movement that happens during various patterns of the clock beats.

$$Pd = Cs\,(Vcc)^2 f_{clk}$$

Where the cumulative value of switching clock is denoted as Cs and f_clk mentioned the frequency of clocking to reduce the dynamic power ‘Pd’ and Vcc denoted as power supply utility to the module.

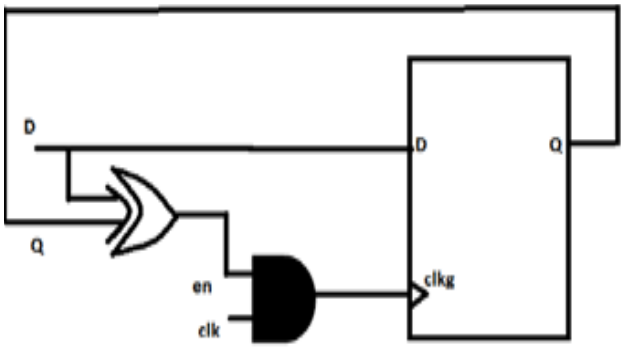

Figure5. Block diagram of improved clock gating with D-FF

The Clock gating wit DFF is given in the figure5. Setup time and hold time are continually influenced by their contributions as long as empower signal is affirmed. They are empowered, their substance changes promptly when their sources of info change. Flip-flops, then again, have their content change just either at the rising or falling edge of the empower signal. This empower signal is normally the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remaining parts steady even.

III. RESULTS AND DISCUSSION

Thus the design model of SRAM and sequential logic of counter circuit is effective utilization. Modification in clock gating technique reduces the leakage power than traditional approaches. The module comprises of one 8-input combinational logic-into table with four devoted registers and is viewed as a major structure of FPGA block.

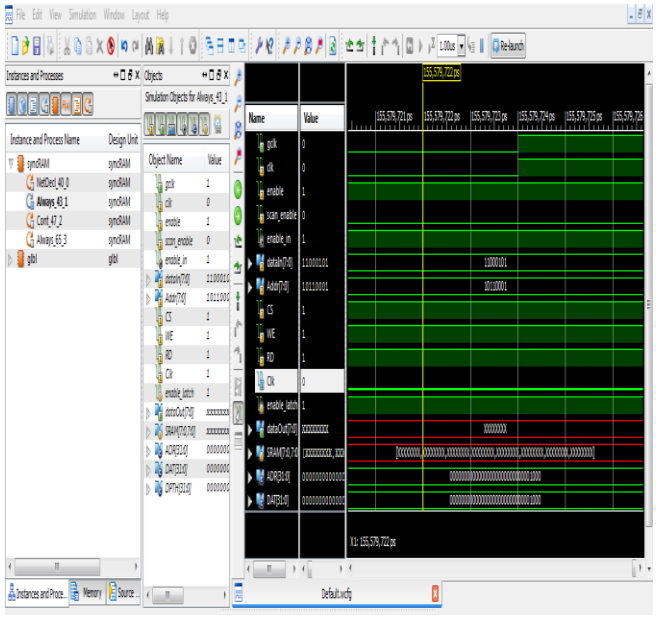

Figure6. Simulation result of SRAM circuit

The simulation result of SRAM is shown in figure 6. Here the gated clock is generated and determines the better utility of performance. The –bit utilization memory is constructed to improve the synchronous logics and it is clock gating is improved the performance of area and delay utility. Here the Table 1 and 2 shows the results of area and delay.

Table1: Area utility of SRAM logic with power optimization strategy

SRAM-Device utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Slice Registers	9	93,120	1%
Slice LUTs	6	46,560	1%
Number used as logic	2	46,560	1%
Number used as Memory	4	16,720	1%
Number of occupied Slices	3	11,640	1%
Number with an	1	6	16%

unused Flip Flop			
No. of fully used LUT-FF pairs	5	6	83%
slice register sites lost to control set restrictions	7	93,120	1%
Bonded IOBs	27	240	11%
BUFG/BUFGCTRLs	2	32	6%

Table2: Delayreport

Parameters of delay	**Value**
Minimum period:	1.257ns
Input arrival time before clock with maximum delay utility	1.324ns
Output required time after clock – maximum reach	1.148ns
path delay - gclk	0.935ns
Clock period	1.257ns
Net delay	0.533ns

The power analysis is the major concern in proposed logic, which utilizes the better utilization on the synchronous RAM with XPower Analyzer tool in Xilinx ISE. Both Static and dynamic power is analyzed with the voltage and current utility, which is shown in the figure7. When the register activity is TURN OFF, the input data need to register the gated clock and clock gets OFF state. The enable and clock applied on the register block, this is the enable clock gating signal.

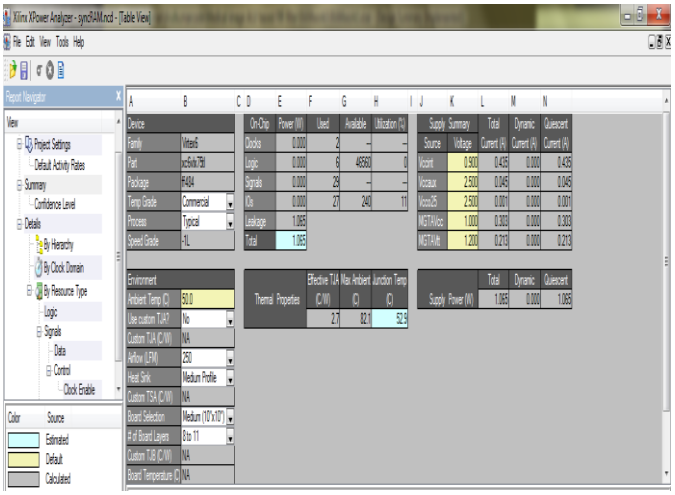

Figure7. XPower analyzer result of SRAM

Sequential circuit power reduction is determined the power, area and delay. The ISim result of sequential logic with bidirectional counter is designed and it is shown in figure8.

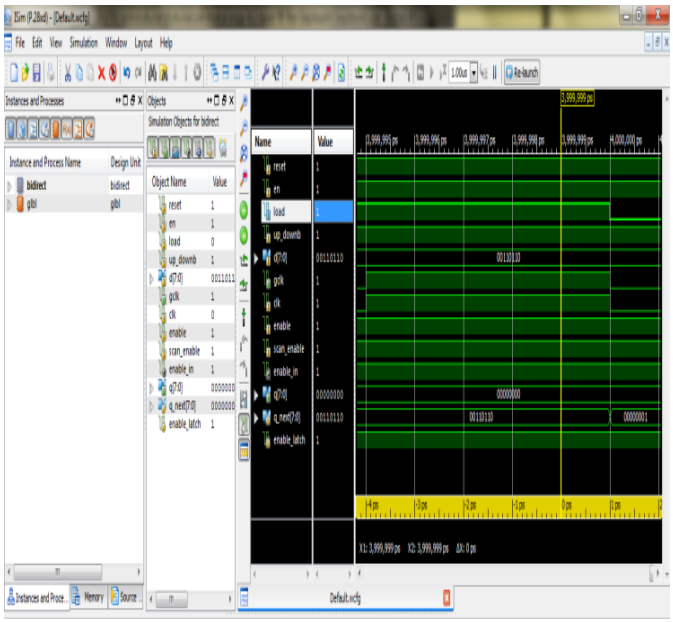

Figure8. Simulation result of Bidirectional counter with power optimal strategy

Table3: Device utilization of bidirectional-counter circuit

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	9	93,120	1%
Number of Slice LUTs	11	46,560	1%
Number used as logic	11	46,560	1%
Number used as Memory	0	16,720	0%
Number of occupied Slices	5	11,640	1%
Number with an unused Flip Flop	2	11	18%
Number with an unused LUT	0	11	0%
Number of fully used LUT-FF pairs	9	11	81%
Number of slice register sites lost to control set restrictions	7	93,120	1%
Number of bonded IOBs	24	240	10%
Number of BUFG/BUFGCTRLs	1	32	3%

Device utilization summary determines the utility of area, which is given in the table 3. Various delays like path delay, net delay and gate delays are analyzed and it is given in the table 4.

Table4: Delay report of sequential circuit

Parameter	Value
gclk	5.859ns
Clk	1.765ns
input arrival time before clock	1.551ns
Maximum output required time after clock	1.148ns
Maximum combinational path delay	0.935ns
Net delay	1.244ns

Bidirectional counter circuit uses the improved clock gating technique for power analysis, which is shown in the figure9. Shifting and DFF register utilities are the major logic block of RTL view. Clock pair shared flip flop based logic, low-swing DFF based logic and gated model of SRAM designs are compared to the proposed logic and it achieves the best result for proposed power reduction technique, which are shown in table 5.

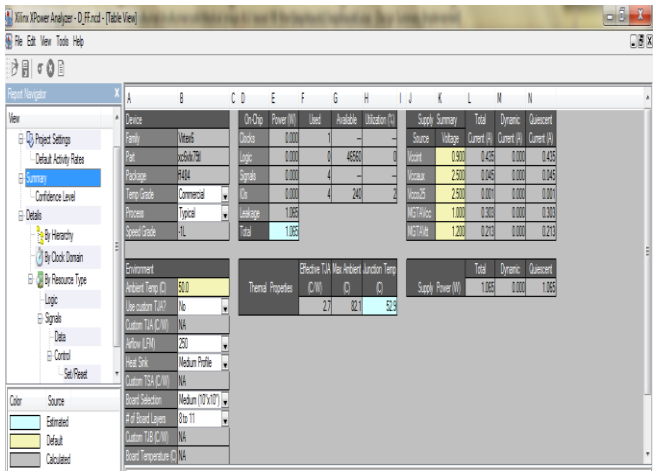

Figure9. XPower analyzer report of Sequential circuit

Table5. Comparison results

Experiment	Power (mW)	Delay(ns) [25]
Existing LSDFF based logic [17]	26.3	52
Existing CPSFF-with Pass transistor logic [17]	14.2	68

Existing - Gated Vdd methodology [7]	63	112
Proposed power reduction logic	1.065	6

In latch based clock gating procedure, a sensitive latch is utilized as the control component, to control the Enable pin, that is taken care of to the "AND" "OR" gate level for gating the clock signal. This latch is permitted to mirror the difference in Enable pin. The clock holds the estimation of empower signal from the dynamic edge of the clock till the idle edge of the clock. In the event that the "AND" is utilized for circuits working on certain edge of clock pulse. Therefore, the proposed clock gating based SRAM and Sequential circuit improves the result of area, delay and power than existing work.

IV. CONCLUSION AND FUTURE SCOPE

Thus it conclude that the design logic of SRAM and sequential counter circuit is improved the performance using improved clock gating technique. Here the power reduction strategy is performed with D-Latch based clock switching with triggering of RTL module in improved clock gating technique.The consequence of this kind of clock gating procedure on a D flip failure is as appeared. Power improvement, generally consigned to the combination, and situation and directing stages, has climbed to the System level also, RTL. HDL can thus utilize clock gating to turn off idle segments of the plan and decrease generally speaking dynamic power utilization. Thus the RTL view of gate level examination determines the better result of SRAM and sequential Bidirectional counter circuit using improved clock gating approach. In future, the work may extend with the voltage limiting and managing approach for power reduction.

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