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A High-Performance Mixed-Logic 4-16 Decoder Designed Using the GDI Technique

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Abstract

The safety and integrity of the data being sent wirelessly should always come first. The primary goal in the development of the decoders was to provide standardized encryption and decryption methods, with the secondary aim of ensuring the confidentiality of data transmissions. Audio systems rely on decoders to convert analog signals to digital data. It acts as a decompressor, allowing compressed media like movies and images to be restored to their uncompressed state. Decoders are electronic circuit-based devices that take computer instructions and generate CPU control signals. There was already a plan for making a 4-16 line decoder, and it included combining two 2-4 decoders. These decoders' outputs were wired into the inputs of fifteen CMOS NAND gates. TGL and DVL logic are used throughout the design process of 2-4 decoders. Now we are going to change these CMOS NAND gates such that they are replaced with GDI logic, which stands for gate diffusion induced logic. The other logic will stay the same. PYXIS GDK 130nm technology is able to be used in the production of this design (MENTOR GRAPHICS). In terms of switching energy, latency, and power-delay product, the decoder outperforms the previously used decoder.

Keywords: This index includes such diverse concepts as complementary metal-oxide semiconductor NAND, 2-4 decoder, transmission gate logic, dual value logic, and gate diffusion induced.

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INTRODUCTION

Having numerous inputs and many outputs, a binary decoder is a combinational circuit. It accepts an n-line binary input and outputs a code with one of 2n possible values. You'll need these parts if your n-bit input value must trigger exactly one of the 2n outputs. The decoded output may be engaged in response to data inputs through enable inputs, which are often present in decoders. Architectural, circuit, layout, and process technology levels may all be used to cater to the rising need for low-power very large scale integration (VLSI).Choosing the appropriate logic style before constructing combinational circuits may save a substantial amount of energy during the circuit construction process. This is because all the major elements that determine power use, latency, and area are significantly influenced by the chosen logic type. The application, the kind of circuit to be implemented, and the design technique all have an impact on the performance considerations that need to be made. This makes it difficult, if not impossible, to establish universally applicable guidelines for the best forms of reasoning. Instead, the research on low-power logic types that has been published so far has focused on specialized logic cells like Decoders, which are used in particular data transit. This research extends these assessments to an extremely wide variety of logic gates, and therefore to arbitrarily complex decoders. To compare the commonalities in power consumption across the many distinct logic types now in use, we utilize both real-world implementations of logic gates and simulations run under realistic circuit topologies and operational circumstances. Studies of sequential elements, such as latches and flip-flops, were not performed but may be found elsewhere in the literature.

There are a number of different logic styles that may be used to construct logic circuits. One kind of logic that may be utilized to create combinational circuits is known as complementary CMOS logic style [3]. In situations when saving energy and minimizing power delays are paramount, this reasoning is used. The CPL is almost twice as fast as conventional CMOS because to its decreased input capacitance and enhanced logic capabilities. When compared to standard CMOS logic, complementary pass transistor logic halves the delay [4]. As an alternative to complementary metal-oxide semiconductor (CMOS) logic, this form of logic exists. To enhance the efficiency of the design as a whole, [5] created an ALU that relies on double-pass transistors.

For both the switching states of MOS transistors and the signals in combinational circuits, [6] makes use of switching and binary signal algebra. The new pass transistor logic, DVL,

matches the performance of its DPL predecessor while using fewer transistors. The latency and power consumption of this logic are significantly reduced [7]. According to certain sources[not in citation given] A method for synthesizing networks like those described above is also developed and shown in this paper. Both speed and efficiency are hallmarks of the new logic.

The benefits of adopting a GDI-based approach (transmission port) for the construction of a low-power combinational logic circuit on static CMOS (SC) implementation and pass transistor logic (PTL), especially in terms of energy consumption and latency, were examined in depth. The complexity of the area is also laid out in [1].

The current design makes use of CMOS, transmission gate logic, and DVL logic techniques. The modified decoder design may tighten the design's constraints when utilized to create Dual Value Logic, Transmission gate logic, and Gate Diffusion Induced logic. Taking use of the decoder's architecture allows for the implementation of such logics. When compared to both the current architecture and the usual CMOS design, the GDI logic type offers lower power requirements and lower latency.

II. MODIFIEDDECODERARCHITECTURE

Digital systems employ binary codes to represent data in discrete increments of data. As many as 2n distinct pieces of information may be represented by an n-bit binary code. If the n-bit coded information includes unused possibilities, a decoder is a combinational circuit that turns the binary information from n input lines into 2n or fewer distinct output lines. A decoder may also take binary data from n input lines and output it in a manner where there are less than 2n distinct lines. These circuits, called n-to-m line decoders, are designed to generate m = 2n min-terms from n input variables. The technical term for these converters is "n-to-m line decoders."

Below, we discovered a 4-16 low-level decoder constructed from two 2-4 decoders and fifteen NAND gates. Using the inputs a, b, c, and d, this decoder will generate the 16 min-terms d0-d15. Using this method, the structure may be divided into two levels. First level may represent up to two 2-4 line decoders' worth of outputs, or eight lines in all. As can be seen in the image below, the outputs from level 1 are linked to the inputs of the 16 NAND gates at level 2.

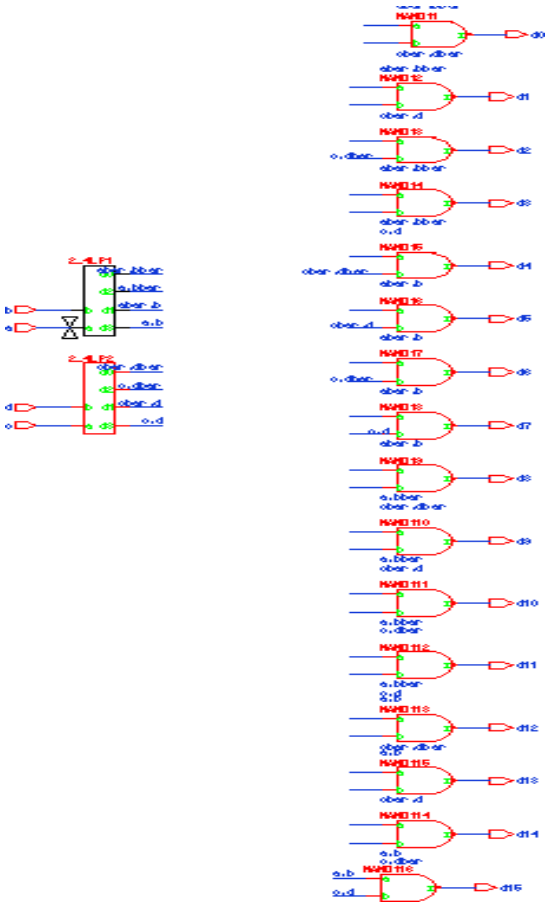


Figure1:ModifieddecoderdesignusingDVL,TGand GDI

A) 2-4 decoder:

A 2-4 line decoder is responsible for the generation of the four minterms D0-D3 of two variables A and B that are input. Table I provides a concise summary of its logical functioning. Depending on the particular combination of inputs, one of the four outputs is chosen and made to have a value of 1, while the other three have values of 0. Due to the fact that an inverted 2-4 decoder produces complimentary minterms I0-I3, the chosen output is set to 0 while the other outputs are all set to 1. This is seen in Table.

Truthtables:2-4DECODER

a) High-leveldecoder

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

b)Low-leveldecoder

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

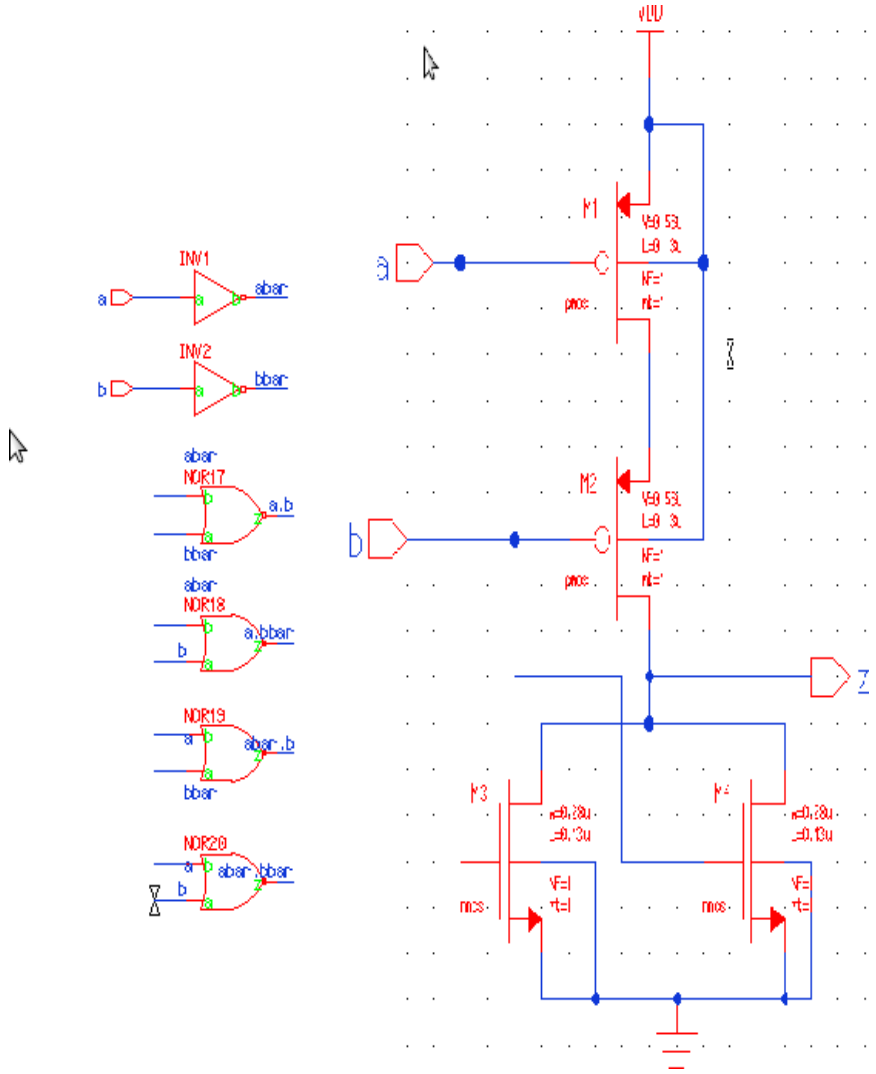
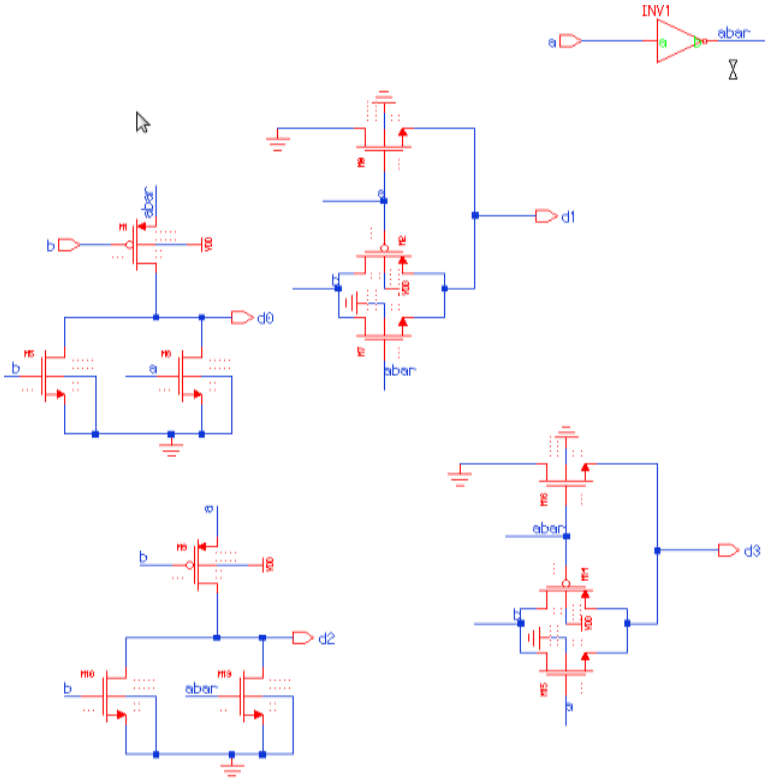


Figure2:CMOSbased 2-4DECODER

The 2-4 decoder architecture shown in figure 2 is based on the CMOS logic shown in figure 1, which already exists in that design. This may be altered [1] by using DVL, which is short for transmission gate logic and can be found in figure 3. The design parameters of latency, energy consumption, and area are all enhanced by the use of these alternative logic techniques. Below is a picture of DVL and TG based logic [1], which may be used in lieu of the 20 transistors needed for this block in a CMOS decoder. We already knew that power consumption is proportional to the number of transistors. The identical 2-to-4 decoder was used in both the original and revised versions of our design. When two 2-4 decodes are added together, eight lines of output are produced. These two decoders are identical other from how their input ports are set up. In this case, we see that there are 16 possible permutations based

on four distinct inputs. These combinations are sent into the inputs of the 16 NAND gates that are being used. When we were working on the improved design, our primary attention was on the NAND gates. The existing design makes use of a CMOS-based NAND gate that has had the logic style known as gate diffusion induced (GDI) changed. The design makes the most of the limitations in the best possible way. Figures 4 and 5, respectively, in the following table illustrate CMOS and GDI-based NAND gates.



In Figure 3, we can see the B) NAND gate design for a DVL and TG-based 2-4 DECODER.

Each of the two NAND gates uses four transistors in total. The link between PMOS and NMOS transistors is the fundamental dividing line between the two types. One features a pull-up to pull-down setup, while the other has two stacked blocks. Connecting the first block's output to the second block's NMOS transistor's source boosts the circuit's efficiency.

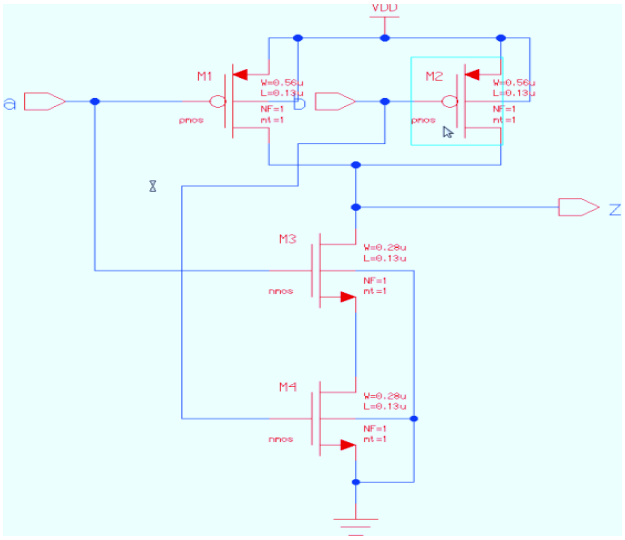
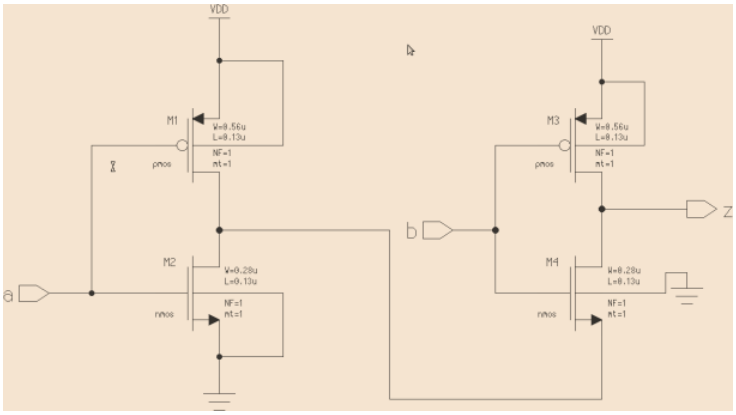


Figure4:CMOSbasedNANDgate



(ii)GDIbasedNAND

PERFORMANCEEVALUTION

In figure 1, the existing NAND gate has been upgraded to a CMOS NAND. This upgrade affects the decoder for bits 4-16. The CMOS logic approach is used throughout the whole of the existing design1 implementation. The second existing design uses DVL for its implementation, and the TG logic used in the 2-4 decoders are created using a CMOS logic approach. To complete the NAND gates, DVL was used. The DVL and TG logic styles were used to construct the 2-4 decoders in the revised design, while the GDI logic style was used to construct the NAND gates. Different supply and input voltages reveal three diverse designs in latency, power consumption, and power delay. Voltages might vary anywhere from 0.4 to 0.8 volts in this example. Figure 6 shows that there are 16 distinct data outputs that may be

detected for each of the 16 possible input combinations. The revised plan yields much improved outcomes, as seen in the tables below.

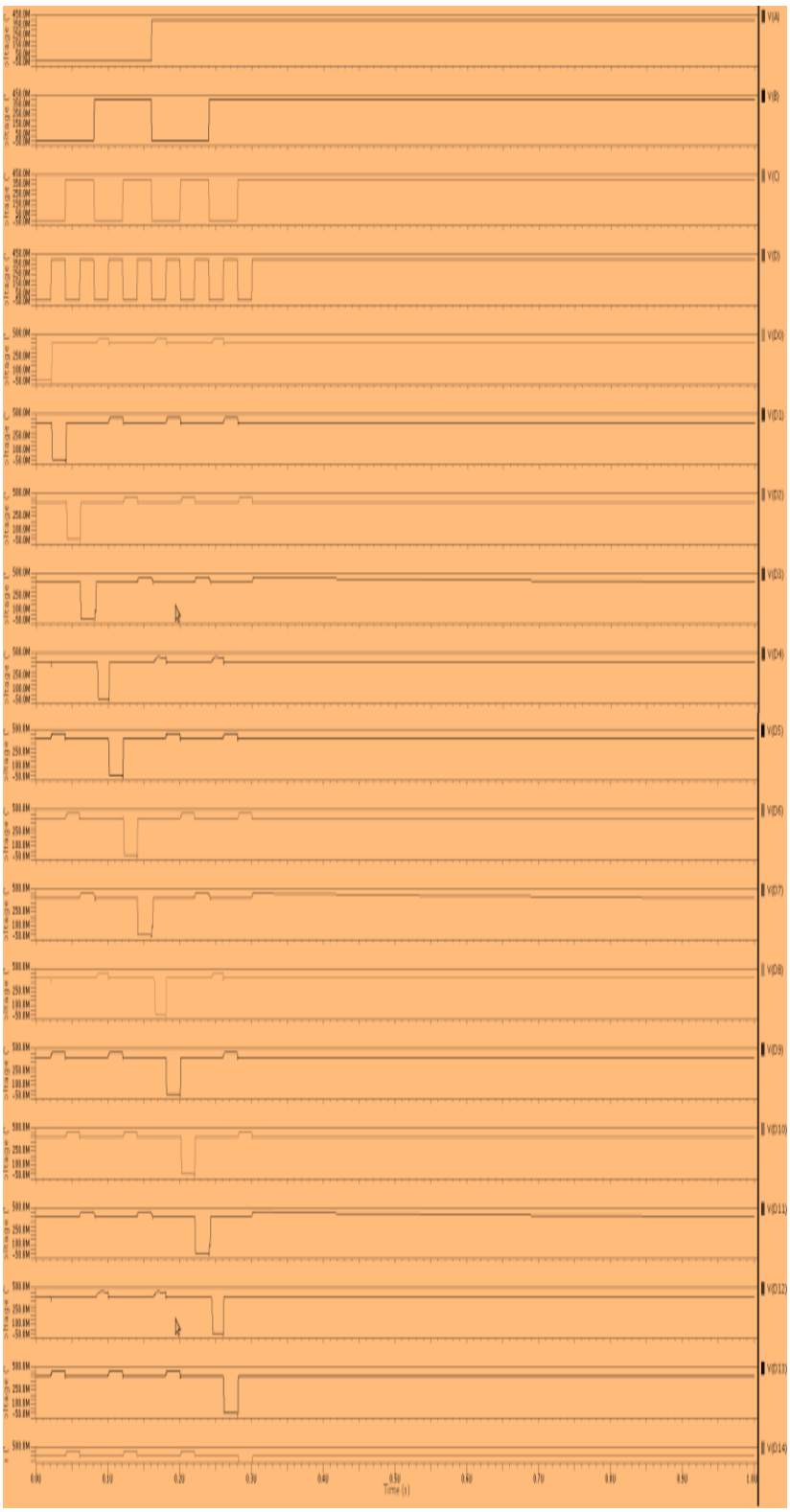


Figure6:output waveformofmodified4-16decoder

TABLE 1: Comparison of New and Old 4-16 Line Decoders for Power Consumption

Designs	Vdd=Vgs=0.9V	Vdd=Vgs=0.7V	Vdd=Vgs=0.6V	Vdd=Vgs=0.5V	Vdd=Vgs=0.4V
Modified(TGL,DVL,GDI)	122.41nW	825.53nW	63.458nW	43.548nW	27.874nW
Existed (TGL, DVL,CMOS)	122.87nW	83.685nW	63.544nW	41.419nW	27.072nW
CMOS	24.39uW	14.278uW	6.517uW	1.560uW	388.56uW

TABLE2:Delayanalysisbetween modifiedand existed 4-16 lineDecoders

Designs	Vdd=Vgs=0.8V	Vdd=Vgs=0.7V	Vdd=Vgs=0.6V	Vdd=Vgs=0.5V	Vdd=Vgs=0.4V
Modified(TGL,DVL,GDI)	632.11Ps	691.77Ps	805.78Ps	2.0139ns	3.2855ns
Existed (TGL, DVL,CMOS)	664.14Ps	733.44Ps	874.21Ps	2.1503ns	3.7170ns
CMOS	640.27Ps	816.06Ps	2.0316ns	2.7951ns	5.2008ns

TABLE3:Power-DelayProductanalysisbetweenmodifiedand existed4-16lineDecoders

Designs	Vdd=Vgs=0.8V	Vdd=Vgs=0.7V	Vdd=Vgs=0.6V	Vdd=Vgs=0.5V	Vdd=Vgs=0.4V
Modified(TGL,DVL,GDI)	59.761×11-24	48.834×11-24	43.312×11-24	43.363×11-18	66.22×11-18
Existed (TGL, DVL,CMOS)	63.725×11-24	53.630×11-24	48.324×11-24	50.028×11-18	79.043×11-24
CMOS	12.587×11-21	8.949×11-21	5.70×11-15	3.196×11-15	1.624×11-24

CONCLUSION

The purpose of this article is to improve the speed and low-levelsumption of a 4-16 low level line decoder, as shown in the preceding tables. With the help of MENTORGRAPHICS' 130nm GDK technology, the full set of design parameters for the Armentor GRAPHICS may be achieved [1]. The efficiency of a GDI NAND-based decoder may be substantially greater than that of a CMOS NAND-based 4-16 decoder design. The modified device uses 1nW less power than DVL, TG, and CMOS-based decoder designs while running at 0.4 volts, and 386uw less power than CMOS-based decoder designs. The new design has a delay of only 0.5ns, which is much less than the 1ns, 2ns, and 5ns of the DVL, TG, and CMOS alternatives, respectively. All these factors contribute to the improved performance offered by the revised design compared to the other two alternatives.

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